

# Program at a Glance

## SUNDAY, MAY 24, 2026

|       |   |   |   |  |   |   |   |   |   |   |   |
|-------|---|---|---|--|---|---|---|---|---|---|---|
| 08:00 | Registration (8:00 AM-18:00 PM)<br>Convention Center Lobby, SHICC, Level 1  |   |   |  |   |   |   |   |   |   |   |
| 08:30 | <b>T1 - From Circuits to Startups: Translating Innovation into Impact (Entrepreneurship Tutorial)</b><br>Conference Room: 5B+5C, SHICC, Level 5 | <b>T2 - AI-Enhanced Implementation of High-Efficiency Delta-Sigma ADCs</b><br>Conference Room: 5H, SHICC, Level 5   | <b>T5 - CoDeCAS: Co-designing Devices, Circuits, Systems and Algorithms for Uncertainty aware Multimodal Artificial Intelligence at the Edge</b><br>Conference Room: Yangtze River Hall, SHICC, Level 5 | <b>T6 - Power electronic circuits-based safety enhancement techniques for lithium-ion batteries</b><br>Conference Room: 5F, SHICC, Level 5 | <b>T7 - High-Throughput Neural Signal Acquisition: Hardware Implementation and Bio-Inspired Approaches</b><br>Conference Room: 5A, SHICC, Level 5 | <b>T8 - Advancing Spatial Intelligence — Geometric Modeling, Representation Learning, and 3D Compression</b><br>Conference Room: 5I, SHICC, Level 5 | <b>T9 - From SNNs to Silicon: Automated hardware deployment of spiking neural networks</b><br>Conference Room: 5D+5E, SHICC, Level 5          | <b>T16 - Mm-Wave to THz Signal Generation in CMOS: An Injection Locking Approach</b><br>Conference Room: 5J, SHICC, Level 5                                 | <b>Standard Workshop</b><br>Conference Room: 3A, SHICC, Level 3 |   | <b>Workshop of the Cryo-Electronics for Quantum Systems and HPC (Cryo4QHPC) Special Interest Group</b><br>Conference Room: 3D, SHICC, Level 3 |
| 09:00 |   |   |   |  |   |   |   |   |   |   |   |
| 09:30 |   |   |   |  |   |   |   |   |   |   |   |
| 10:00 | Coffee Break<br>Room: Convention Center Lobby, SHICC, Level 5   |   |   |  |   |   |   |   |   |   |   |
| 10:30 | <b>T1 - From Circuits to Startups: Translating Innovation into Impact (Entrepreneurship Tutorial)</b><br>Conference Room: 5B+5C, SHICC, Level 5 | <b>T2 - AI-Enhanced Implementation of High-Efficiency Delta-Sigma ADCs</b><br>Conference Room: 5H, SHICC, Level 5   | <b>T5 - CoDeCAS: Co-designing Devices, Circuits, Systems and Algorithms for Uncertainty aware Multimodal Artificial Intelligence at the Edge</b><br>Conference Room: Yangtze River Hall, SHICC, Level 5 | <b>T6 - Power electronic circuits-based safety enhancement techniques for lithium-ion batteries</b><br>Conference Room: 5F, SHICC, Level 5 | <b>T7 - High-Throughput Neural Signal Acquisition: Hardware Implementation and Bio-Inspired Approaches</b><br>Conference Room: 5A, SHICC, Level 5 | <b>T8 - Advancing Spatial Intelligence — Geometric Modeling, Representation Learning, and 3D Compression</b><br>Conference Room: 5I, SHICC, Level 5 | <b>T9 - From SNNs to Silicon: Automated hardware deployment of spiking neural networks</b><br>Conference Room: 5D+5E, SHICC, Level 5          | <b>T16 - Mm-Wave to THz Signal Generation in CMOS: An Injection Locking Approach</b><br>Conference Room: 5J, SHICC, Level 5                                 | <b>Standard Workshop</b><br>Conference Room: 3A, SHICC, Level 3 |   | <b>Workshop of the Cryo-Electronics for Quantum Systems and HPC (Cryo4QHPC) Special Interest Group</b><br>Conference Room: 3D, SHICC, Level 3 |
| 11:00 |   |   |   |  |   |   |   |   |   |   |   |
| 11:30 |   |   |   |  |   |   |   |   |   |   |   |
| 12:00 | Lunch   |   |   |  |   |   |   |   |   |   |   |
| 12:30 | Lunch   |   |   |  |   |   |   |   |   |   |   |
| 13:00 | Lunch   |   |   |  |   |   |   |   |   |   |   |
| 13:30 | <b>T17 - Efficient Learning-based Models for Multimodal Data Compression</b><br>Conference Room: 5B+5C, SHICC, Level 5                          | <b>T13 - Optical Biotelemetry Systems: Basics and Advances for Wireless Data and Power Transmission in Biomedical Implants</b><br>Conference Room: 5H, SHICC, Level 5 | <b>T11 - Visual Signal Processing from Human to Embodied Intelligence</b><br>Conference Room: Yangtze River Hall, SHICC, Level 5  | <b>T4 - Towards 6G UWB Signal Processing Chain Design</b><br>Conference Room: 5F, SHICC, Level 5   | <b>T15 - Modern Power Amplifier Design: From Classical Principles to AI-Assisted Optimization</b><br>Conference Room: 5A, SHICC, Level 5          | <b>T12 - Intelligent Design of Wireless Power Transfer: From Fundamentals to AI-Driven Frameworks</b><br>Conference Room: 5I, SHICC, Level 5        | <b>T10 - Low-voltage frequency generation, modulation, and demodulation circuits for mobile IoT</b><br>Conference Room: 5D+5E, SHICC, Level 5 | <b>T14 - Leveraging IEEE DataPort and IEEE Data Descriptions for Enhanced Research Impact and Student Engagement</b><br>Conference Room: 5J, SHICC, Level 5 | <b>Standard Workshop</b><br>Conference Room: 3A, SHICC, Level 3 | <b>CASS-CONNECT: Connecting Academia and Industry Workshop</b><br>Conference Room: 3B, SHICC, Level 3 | <b>Workshop of the Cryo-Electronics for Quantum Systems and HPC (Cryo4QHPC) Special Interest Group</b><br>Conference Room: 3D, SHICC, Level 3 |
| 14:00 |   |   |   |  |   |   |   |   |   |   |   |
| 14:30 |   |   |   |  |   |   |   |   |   |   |   |
| 15:00 | Coffee Break<br>Room: Convention Center Lobby, SHICC, Level 5   |   |   |  |   |   |   |   |   |   |   |
| 15:30 | <b>T17 - Efficient Learning-based Models for Multimodal Data Compression</b><br>Conference Room: 5B+5C, SHICC, Level 5                          | <b>T13 - Optical Biotelemetry Systems: Basics and Advances for Wireless Data and Power Transmission in Biomedical Implants</b><br>Conference Room: 5H, SHICC, Level 5 | <b>T11 - Visual Signal Processing from Human to Embodied Intelligence</b><br>Conference Room: Yangtze River Hall, SHICC, Level 5  | <b>T4 - Towards 6G UWB Signal Processing Chain Design</b><br>Conference Room: 5F, SHICC, Level 5   | <b>T15 - Modern Power Amplifier Design: From Classical Principles to AI-Assisted Optimization</b><br>Conference Room: 5A, SHICC, Level 5          | <b>T12 - Intelligent Design of Wireless Power Transfer: From Fundamentals to AI-Driven Frameworks</b><br>Conference Room: 5I, SHICC, Level 5        | <b>T10 - Low-voltage frequency generation, modulation, and demodulation circuits for mobile IoT</b><br>Conference Room: 5D+5E, SHICC, Level 5 | <b>T14 - Leveraging IEEE DataPort and IEEE Data Descriptions for Enhanced Research Impact and Student Engagement</b><br>Conference Room: 5J, SHICC, Level 5 | <b>Standard Workshop</b><br>Conference Room: 3A, SHICC, Level 3 |   | <b>Workshop of the Cryo-Electronics for Quantum Systems and HPC (Cryo4QHPC) Special Interest Group</b><br>Conference Room: 3D, SHICC, Level 3 |
| 16:00 |   |   |   |  |   |   |   |   |   |   |   |
| 16:30 |   |   |   |  |   |   |   |   |   |   |   |
| 17:00 | Lunch   |   |   |  |   |   |   |   |   |   |   |
| 17:30 | Lunch   |   |   |  |   |   |   |   |   |   |   |
| 18:00 | Welcome Reception<br>Room: Pearl Hall & Foyer, Shanghai Min, SHICC, Level 7   |   |   |  |   |   |   |   |   |   |   |
| 21:00 | Welcome Reception<br>Room: Pearl Hall & Foyer, Shanghai Min, SHICC, Level 7   |   |   |  |   |   |   |   |   |   |   |



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# MONDAY, MAY 25, 2026

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|-------|---|--|--|---|--|---|--|--|--|---|---|--|---|--|---|--|--|
| 08:00 | <b>Registration (8:00 AM–18:00 PM)</b><br>Room: Convention Center Lobby, SHICC, Level 1   |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |
| 08:30 | <b>Opening Ceremony</b><br>Conference Room: Grand Ballroom 1, SHICC, Level 7  |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |
| 09:00 | <b>Keynote: New Semiconductor Path in Practice</b><br>Conference Room: Grand Ballroom 1, SHICC, Level 7   |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |
| 09:30 |   |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |
| 10:00 | <b>Coffee Break</b><br>Room: Grand Ballroom 1 Foyer, SHICC, Level 7/Exhibition Area & Poster Gallery, SHICC, Level 3  |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |
| 10:30 | <b>A2L-01</b><br>Modeling, Sensors, and Emerging Analog Systems (5 papers)<br>Chr: Yi Zhong, Nagendra Krishnapura<br>Track: 1<br>Conference Room: 3C, SHICC, Level 3            | <b>A2L-02</b><br>High-Speed Data Converters and Time-Domain ADCs (5 papers)<br>Chr: Tawfiq Musah, Luis Oliveira<br>Track: 1<br>Conference Room: 3I+3J, SHICC, Level 3        | <b>A2L-03</b><br>High-Speed Interface and Wireline Circuits (5 papers)<br>Chr: Navid Yazdi, Yanquan Luo<br>Track: 1<br>Conference Room: 3A, SHICC, Level 3 | <b>A2L-04</b><br>Hardware Security for Internet-of-Things, Cyber-Physical Systems I (5 papers)<br>Chr: Preet Yadav, Yeong-Kang Lai<br>Track: 2<br>Conference Room: 3D, SHICC, Level 3 | <b>A2L-05</b><br>SoC, NoC, Multi-Core, and 3D/2.5D Integrated Circuits and Systems I (5 papers)<br>Chr: Fakhrul Zaman Rokhani, Danella Zhao<br>Track: 2<br>Conference Room: 3E, SHICC, Level 3 | <b>A2L-06</b><br>Post-Quantum Cryptography and High-Speed Links (5 papers)<br>Chr: Dur-e-Shahwar Kundi, Youngjoo Lee<br>Track: 3<br>Conference Room: 3B, SHICC, Level 3 | <b>A2L-07</b><br>Integrated Power Circuits and Charge Pumps (5 papers)<br>Chr: Xiaolu Lucia Li, Yang Jiang<br>Track: 4<br>Conference Room: 3G, SHICC, Level 3                        | <b>A2L-08</b><br>Ferroelectric and Memristive in-Memory Computing (5 papers)<br>Chr: Kyeong-Sik Min, Vasilis Ntinis<br>Track: 5<br>Conference Room: 5C, SHICC, Level 5 | <b>A2L-09</b><br>Spiking Neural Network Architectures and Learning (5 papers)<br>Chr: Qinyu Chen, Xiaofang Pan<br>Track: 8<br>Conference Room: 5F, SHICC, Level 5  | <b>A2L-10</b><br>Image and Vision Sensors I (5 papers)<br>Chr: Ricardo Carmona Galan, Joseph Schmitz<br>Track: 7<br>Conference Room: 5D, SHICC, Level 5                         | <b>A2L-11</b><br>Accelerators for Machine Learning (5 papers)<br>Chr: Walter Leon Salas, Weixiong Jiang<br>Track: 14<br>Conference Room: 5H, SHICC, Level 5                         | <b>A2L-12</b><br>Representation and Compression for Vision and Multimodal Learning Systems (5 papers)<br>Chr: Shiqi Wang, Qingsong Xie<br>Track: 12<br>Conference Room: 5E, SHICC, Level 5 | <b>A2L-13</b><br>Synergies between Emerging AI Technologies and Circuits and Systems (5 papers)<br>Chr: Adam Liu, Yue Zhang<br>Track: 15<br>Conference Room: 5A, SHICC, Level 5   | <b>A2L-14</b><br>AI for Medical Signal and Image Analysis (4 papers)<br>Chr: Mohamad Sawan, Yunshan Zhang<br>Track: 6<br>Conference Room: 5B, SHICC, Level 5 | <b>Poster Session &amp; Live Demo</b><br>Room: SHICC Lobby, Level 3 |  |  |
| 11:00 |   |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |
| 11:30 |   |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |
| 12:00 | <b>Lunch</b><br>Room: Mandarin Hall, SHICC, Level 1   |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |
| 12:30 |   |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |
| 13:00 |   |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |
| 13:30 | <b>Keynote: Unprecedented Vision - From Single photon Detectors and Pixels to Engineering and Health Systems</b><br>Conference Room: Grand Ballroom 1, SHICC, Level 7           |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |
| 14:00 |   |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |
| 14:30 | <b>Coffee Break</b><br>Room: Exhibition Area & Poster Gallery, SHICC, Level 3   |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |
| 15:00 | <b>A4L-01</b><br>AI-Assisted and Emerging Analog Circuits (5 papers)<br>Chr: Gordon Roberts, Liangjian Lyu<br>Track: 1<br>Conference Room: 3C, SHICC, Level 3                   | <b>A4L-02</b><br>Pipeline and Non-Conventional ADC Architectures (5 papers)<br>Chr: Jorge Fernandes, Edoardo Bonizzoni<br>Track: 1<br>Conference Room: 3I+3J, SHICC, Level 3 | <b>A4L-03</b><br>Voltage References and Power Management (5 papers)<br>Chr: Filippo Neri, Bibhu Sahoo<br>Track: 1<br>Conference Room: 3A, SHICC, Level 3   | <b>A4L-04</b><br>Datapath & Arithmetic Circuits and Systems I (5 papers)<br>Chr: Ettore Napoli, Hao Zhang<br>Track: 2<br>Conference Room: 3D, SHICC, Level 3                          | <b>A4L-05</b><br>SoC, NoC, Multi-Core, and 3D/2.5D Integrated Circuits and Systems II (5 papers)<br>Chr: Huiyun Li, Fakhrul Zaman Rokhani<br>Track: 2<br>Conference Room: 3E, SHICC, Level 3   | <b>A4L-06</b><br>Wireless Communications I (5 papers)<br>Chr: Jienan Chen, Shan Cao<br>Track: 3<br>Conference Room: 3B, SHICC, Level 3                                  | <b>A4L-07</b><br>High Efficiency Converters and Drive Circuits for Specialized Applications (5 papers)<br>Chr: Mo Huang, Hui Wang<br>Track: 4<br>Conference Room: 3G, SHICC, Level 3 | <b>A4L-08</b><br>Spintronics-based In-Memory Computing (5 papers)<br>Chr: Hongwu Jiang, Vasilis Ntinis<br>Track: 5<br>Conference Room: 5C, SHICC, Level 5              | <b>A4L-09</b><br>Neuromorphic Circuits and Neuron Implementations (5 papers)<br>Chr: Jim Harkin, Zhenglai Wang<br>Track: 8<br>Conference Room: 5F, SHICC, Level 5  | <b>A4L-10</b><br>Biochemical and Environmental Sensors (5 papers)<br>Chr: Paula Lopez Martinez, Juan Antonio Leñero-Bardallo<br>Track: 7<br>Conference Room: 5D, SHICC, Level 5 | <b>A4L-11</b><br>Circuits, Systems and Architectures for Machine Learning I (5 papers)<br>Chr: Ibrahim Elfadel, Weijie Jiang<br>Track: 14<br>Conference Room: 5H, SHICC, Level 5    | <b>A4L-12</b><br>Architectures and Compression Techniques for Rendering, Perception, and Forecasting (5 papers)<br>Chr: Li Li, Xin Lou<br>Track: 12<br>Conference Room: 5E, SHICC, Level 5 | <b>A4L-13</b><br>Artificial Intelligence in Power and Energy Circuits and Systems I (5 papers)<br>Chr: Herbert Iu, Qing Zhang<br>Track: 15<br>Conference Room: 5A, SHICC, Level 5 | <b>A4L-14</b><br>Bio-Signal Acquisition Front-Ends (5 papers)<br>Chr: Hua Fan, Jiangchao Wu<br>Track: 6<br>Conference Room: 5B, SHICC, Level 5               | <b>Poster Session</b><br>Room: SHICC Lobby, Level 3                 | <b>IEEE CASS Student Design Competition</b><br>Conference Room: Yangtze River Hall, SHICC, Level 5 | <b>Artificial Intelligence Workshop: Foundation Models, Compute Platforms, and Emerging Application</b><br>Conference Room: 5J, SHICC, Level 5 |
| 15:30 |   |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |
| 16:00 |   |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |
| 16:30 | <b>A5L-01</b><br>Programmable, High-Drive, and High-Voltage Amplifiers (5 papers)<br>Chr: Salvatore Pennisi, Gaetano Palumbo<br>Track: 1<br>Conference Room: 3C, SHICC, Level 3 | <b>A5L-02</b><br>Delta-Sigma ADCs and DAC Techniques (5 papers)<br>Chr: Jose de la Rosa, Qiang Li<br>Track: 1<br>Conference Room: 3I+3J, SHICC, Level 3                      | <b>A5L-03</b><br>VCO Design and Oscillator Techniques (5 papers)<br>Chr: Jorge Fernandes, Lei Zhang<br>Track: 1<br>Conference Room: 3A, SHICC, Level 3     | <b>A5L-04</b><br>Datapath & Arithmetic Circuits and Systems II (5 papers)<br>Chr: Hao Zhang, Ettore Napoli<br>Track: 2<br>Conference Room: 3D, SHICC, Level 3                         | <b>A5L-05</b><br>Electronic Design Automation and Physical Design I (5 papers)<br>Chr: Xinfei Guo, Lan-Da Van<br>Track: 2<br>Conference Room: 3E, SHICC, Level 3                               | <b>A5L-06</b><br>Wireless Communications II (5 papers)<br>Chr: Shan Cao, Joungsun Park<br>Track: 3<br>Conference Room: 3B, SHICC, Level 3                               | <b>A5L-07</b><br>Circuits and Systems for Wireless Power Transfer applications (5 papers)<br>Chr: Zhicong Huang, Chi-Seng Lam<br>Track: 4<br>Conference Room: 3G, SHICC, Level 3     | <b>A5L-08</b><br>Quantum Computing I (5 papers)<br>Chr: Georgios Ch. Sirakoulis, Vasilis Ntinis<br>Track: 5<br>Conference Room: 5C, SHICC, Level 5                     | <b>A5L-09</b><br>Grand Challenge on Neural Network-based Video Coding (4 papers)<br>Chr: Li Zhang, Zhipin Deng<br>Track: 17<br>Conference Room: 5F, SHICC, Level 5 | <b>A5L-10</b><br>Sensory Circuits and Systems I (5 papers)<br>Chr: Nicola Massari, Ibrahim Elfadel<br>Track: 7<br>Conference Room: 5D, SHICC, Level 5                           | <b>A5L-11</b><br>Circuits, Systems and Architectures for Machine Learning II (5 papers)<br>Chr: Ricardo Carmona Galan, Biao Pan<br>Track: 14<br>Conference Room: 5H, SHICC, Level 5 | <b>A5L-12</b><br>Multimodal Dialog, Speech Processing, and 3D Representation (4 papers)<br>Chr: Xin Jin, Qingsong Xie<br>Track: 12<br>Conference Room: 5E, SHICC, Level 5                  | <b>A5L-13</b><br>Artificial Intelligence in Power and Energy Circuits and Systems II (5 papers)<br>Chr: Herbert Iu, Miao Meng<br>Track: 15<br>Conference Room: 5A, SHICC, Level 5 | <b>A5L-14</b><br>Medical Computing Hardware and SoCs (5 papers)<br>Chr: Jie Chen, Cheng Han<br>Track: 6<br>Conference Room: 5B, SHICC, Level 5               |   |  |  |
| 17:00 |   |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |
| 17:30 |   |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |
| 18:00 | <b>WICAS-YPCAS Event</b>  |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |
| 21:30 | Room: Europe Hall, SHICC, Level 5   |  |  |   |  |   |  |  |  |   |   |  |   |  |   |  |  |

# TUESDAY, MAY 26, 2026

**Registration (8:00 AM-18:00 PM)**  
Room: Convention Center Lobby, SHICC, Level 1

**Kirchhoff and IEEE CASS Awards**  
Conference Room: Grand Ballroom 1, SHICC, Level 7

**Keynote: Quantum Network: Quantum Communication, Computation, and Metrology**  
Conference Room: Grand Ballroom 1, SHICC, Level 7

**Coffee Break**  
Room: Exhibition Area & Poster Gallery, SHICC, Level 3

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|-------|--|---|--|---|--|--|--|--|--|--|--|--|---|--|--|--|
| 10:00 |  |   |  |   |  |  |  |  |  |  |  |  |   |  | Poster Session & Live Demo<br>Room: SHICC Lobby, Level 3 |  |
| 10:30 | <b>B2L-01</b><br>RF Frequency Generation and Synthesizers (4 papers)<br>Chr: Xi Zhu, Arindam Sanyal<br>Track: 1<br>Conference Room: 3C, SHICC, Level 3 | <b>B2L-02</b><br>Time-Interleaved and High-Speed SAR ADCs (5 papers)<br>Chr: Yi Shen, Hyeon Kim<br>Track: 1<br>Conference Room: 3I+3J, SHICC, Level 3 | <b>B2L-03</b><br>Oscillators, PLLs, and Clock Generation (5 papers)<br>Chr: Filippo Neri, Degang Chen<br>Track: 1<br>Conference Room: 3A, SHICC, Level 3 | <b>B2L-04</b><br>Hardware Security for Logic, Circuits and Architectures I (5 papers)<br>Chr: Martinez Alonso Abdel, Jing Tian<br>Track: 2<br>Conference Room: 3D, SHICC, Level 3 | <b>B2L-05</b><br>Electronic Design Automation and Physical Design II (5 papers)<br>Chr: Bruce Sham, Kun-Chih Chen<br>Track: 2<br>Conference Room: 3E, SHICC, Level 3 | <b>B2L-06</b><br>Wireline Communications I (5 papers)<br>Chr: Yuan Du, Xinpeng Xing<br>Track: 3<br>Conference Room: 3B, SHICC, Level 3 | <b>B2L-07</b><br>Circuits and Systems for Enhanced DC-DC Switch-mode Power Supplies (5 papers)<br>Chr: Yang Jiang, Yanzhao Ma<br>Track: 4<br>Conference Room: 3G, SHICC, Level 3 | <b>B2L-08</b><br>AI Circuits and Architectures (5 papers)<br>Chr: Ronald Tetzlaff, Wai-Chi Fang<br>Track: 5<br>Conference Room: 5C, SHICC, Level 5 | <b>B2L-09</b><br>Compute-in-Memory-Based Neural Computing (5 papers)<br>Chr: Di He, Yuqi Su<br>Track: 8<br>Conference Room: 5F, SHICC, Level 5 | <b>B2L-10</b><br>Sensory Signal Conditioning (5 papers)<br>Chr: Mario Renteria Pinon, Yan Liu<br>Track: 7<br>Conference Room: 5D, SHICC, Level 5 | <b>B2L-11</b><br>Quantization, Approximation, and Compression for ML Hardware I (5 papers)<br>Chr: Milin Zhang, Shiwei Liu<br>Track: 14<br>Conference Room: 5H, SHICC, Level 5 | <b>B2L-12</b><br>Multimodal Interfaces and Efficient Architectures for Intelligent Visual Systems (4 papers)<br>Chr: Weiyao Lin, Lei Qiu<br>Track: 12<br>Conference Room: 5E, SHICC, Level 5 | <b>B2L-13</b><br>Empowering the Evolving Electrical Grid: Circuits & Systems for Greener Generation, Distribution I (5 papers)<br>Chr: Federico Bizzarri, C. K. Michael Tse<br>Track: 15<br>Conference Room: 5A, SHICC, Level 5 | <b>B2L-14</b><br>Neural Recording and Stimulation ASICs (5 papers)<br>Chr: Sohyung Ha, Tim Constandinou<br>Track: 6<br>Conference Room: 5B, SHICC, Level 5 |  |  |
| 11:00 |  |   |  |   |  |  |  |  |  |  |  |  |   |  |  |  |
| 11:30 |  |   |  |   |  |  |  |  |  |  |  |  |   |  |  |  |

**Lunch**  
Room: Mandarin Hall, SHICC, Level 1

**Keynote: Taming the Dragon: Circuits and Systems for Energy-efficient and Secure Computation**  
Conference Room: Grand Ballroom 1, SHICC, Level 7

**Coffee Break**  
Room: Exhibition Area & Poster Gallery, SHICC, Level 3

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| 14:30 |   |   |   |   |   |   |   |  |  |   |   |  |  |  | Poster Session<br>Room: SHICC Lobby, Level 3 | Industry Forum I: AI-Driven Innovation for the Future Chip Design<br>Conference Room: Grand Ballroom 1, SHICC, Level 7 | Industry Forum II: Charting the Next Era of Semiconductors<br>Conference Room: Yellow River, SHICC, Level 3 | IEEE CASS Chapter Leadership Workshop @ ISCAS 2026 (Shanghai)<br>Conference Room: 5I, SHICC, Level 5 |
| 15:00 | <b>B4L-01</b><br>RF and mm-Wave Low-Noise Amplifiers (5 papers)<br>Chr: Raafat Labadibi, Luis Oliveira<br>Track: 1<br>Conference Room: 3C, SHICC, Level 3   | <b>B4L-02</b><br>Delta-Sigma and Zoom ADCs (5 papers)<br>Chr: Qiang Li, Jose de la Rosa<br>Track: 1<br>Conference Room: 3I+3J, SHICC, Level 3                                   | <b>B4L-03</b><br>Multiphase PLLs and Injection-Locked Clocks (5 papers)<br>Chr: Shahriar Mirabbasi, Robert Sobot<br>Track: 1<br>Conference Room: 3A, SHICC, Level 3 | <b>B4L-04</b><br>Hardware Security for Logic, Circuits and Architectures II (5 papers)<br>Chr: Martinez Alonso Abdel, Xiaojin Zhao<br>Track: 2<br>Conference Room: 3D, SHICC, Level 3 | <b>B4L-05</b><br>Electronic Design Automation and Physical Design III (5 papers)<br>Chr: Xinfei Guo, Tony Tae-Hyoung Kim<br>Track: 2<br>Conference Room: 3E, SHICC, Level 3 | <b>B4L-06</b><br>Homomorphic Encryption and Quantum Circuits (5 papers)<br>Chr: Xinpeng Xing, Hanho Lee<br>Track: 3<br>Conference Room: 3B, SHICC, Level 3  | <b>B4L-07</b><br>Circuits & Systems for Energy Harvesting I (5 papers)<br>Chr: Junrui Liang, Jinbo Li<br>Track: 4<br>Conference Room: 3G, SHICC, Level 3          | <b>B4L-08</b><br>Nanoelectronic Circuits (5 papers)<br>Chr: Feng Zhang, Georgios Ch. Sirakoulis<br>Track: 5<br>Conference Room: 5C, SHICC, Level 5 | <b>B4L-09</b><br>Neuromorphic Processor Architecture and System (5 papers)<br>Chr: Yuncheng Lu, Xinming Shi<br>Track: 8<br>Conference Room: 5F, SHICC, Level 5 | <b>B4L-10</b><br>Machine Learning for Signal Processing (5 papers)<br>Chr: Yudong Zhang, Xin Lou<br>Track: 10<br>Conference Room: 5D, SHICC, Level 5                  | <b>B4L-11</b><br>Compute-in-Memory I (5 papers)<br>Chr: Peilin Liu, Zhiting Lin<br>Track: 14<br>Conference Room: 5H, SHICC, Level 5       | <b>B4L-12</b><br>Computational Intelligence for Multimedia Understanding (4 papers)<br>Chr: Maria Trocan, Behçet Uğur Töreyn<br>Track: 18<br>Conference Room: 5E, SHICC, Level 5 | <b>B4L-13</b><br>Empowering the Evolving Electrical Grid: Circuits & Systems for Greener Generation, Distribution II (4 papers)<br>Chr: Federico Bizzarri, C. K. Michael Tse<br>Track: 15<br>Conference Room: 5A, SHICC, Level 5 | <b>B4L-14</b><br>Sensing Interfaces and SoCs (5 papers)<br>Chr: Pantelis Georgiou, Changgui Yang<br>Track: 6<br>Conference Room: 5B, SHICC, Level 5      |  |  |   |  |
| 15:30 |   |   |   |   |   |   |   |  |  |   |   |  |  |  |  |  |   |  |
| 16:00 |   |   |   |   |   |   |   |  |  |   |   |  |  |  |  |  |   |  |
| 16:30 | <b>B5L-01</b><br>RF and mm-Wave Transceivers and Receivers (5 papers)<br>Chr: Jerald Yoo, Arindam Sanyal<br>Track: 1<br>Conference Room: 3C, SHICC, Level 3 | <b>B5L-02</b><br>Noise-Shaping ADCs and DAC Techniques for SAR ADCs (5 papers)<br>Chr: Jorge Fernandes, Gonçalo Rodrigues<br>Track: 1<br>Conference Room: 3I+3J, SHICC, Level 3 | <b>B5L-03</b><br>Advanced Analog and Mixed-Signal Techniques I (5 papers)<br>Chr: Randall Geiger, Ankesh Jain<br>Track: 1<br>Conference Room: 3A, SHICC, Level 3    | <b>B5L-04</b><br>Hardware Security for Logic, Circuits and Architectures III (4 papers)<br>Chr: Xiaojin Zhao, Chia Sun<br>Track: 2<br>Conference Room: 3D, SHICC, Level 3             | <b>B5L-05</b><br>Programmable, Reconfigurable & Array Architectures I (5 papers)<br>Chr: Danella Zhao, Chung-An Shen<br>Track: 2<br>Conference Room: 3E, SHICC, Level 3     | <b>B5L-06</b><br>AI/ML for Communication and Signal Processing (4 papers)<br>Chr: Youngmin Kim, Shan Cao<br>Track: 3<br>Conference Room: 3B, SHICC, Level 3 | <b>B5L-07</b><br>Circuits & Systems for Energy Harvesting II (5 papers)<br>Chr: Junrui Liang, Xiongchuan Huang<br>Track: 4<br>Conference Room: 3G, SHICC, Level 3 | <b>B5L-08</b><br>Quantum Computing II (5 papers)<br>Chr: Hao Cai, Feng Zhang<br>Track: 5<br>Conference Room: 5C, SHICC, Level 5                    | <b>B5L-09</b><br>Neuromorphic Learning and Plasticity (5 papers)<br>Chr: Qinyu Chen, Lianbo Wu<br>Track: 8<br>Conference Room: 5F, SHICC, Level 5              | <b>B5L-10</b><br>Signal Processing Theories and Algorithms for Biosignals (4 papers)<br>Chr: Wei Liu, Weihao Wang<br>Track: 10<br>Conference Room: 5D, SHICC, Level 5 | <b>B5L-11</b><br>Compute-in-Memory II (5 papers)<br>Chr: Kannaujya Aryan, Liang Chang<br>Track: 14<br>Conference Room: 5H, SHICC, Level 5 | <b>B5L-12</b><br>Circuits and Systems for Coding and Processing (5 papers)<br>Chr: Heming Sun, Hui Zhang<br>Track: 11<br>Conference Room: 5E, SHICC, Level 5                     | <b>B5L-13</b><br>Specialized Hardware for Embodied AI Application and Neuromorphic Computing I (5 papers)<br>Chr: Yueting Li, Bo Li<br>Track: 15<br>Conference Room: 5A, SHICC, Level 5  | <b>B5L-14</b><br>Wireless Power and Implantable Systems (5 papers)<br>Chr: Arindam Basu, Hanjun Jiang<br>Track: 6<br>Conference Room: 5B, SHICC, Level 5 |  |  |   |  |
| 17:00 |   |   |   |   |   |   |   |  |  |   |   |  |  |  |  |  |   |  |
| 17:30 |   |   |   |   |   |   |   |  |  |   |   |  |  |  |  |  |   |  |

**Gala Dinner & ISCAS Awards Ceremony**  
Conference Room: Grand Ballroom 1, SHICC, Level 7

18:00  
19:00  
21:00

# WEDNESDAY, MAY 27, 2026

**Registration (8:30 AM~13:00 PM)**  
Room: Convention Center Lobby, SHICC, Level 1

**Keynote: From Memory-Constrained to Memory-Optimized: How Engram Conditional Memory + MRDIMM/CXL Reshapes Sparse AI Architectures**  
Conference Room: Grand Ballroom 1, SHICC, Level 7

**Coffee Break**  
Room: Exhibition Area & Poster Gallery, SHICC, Level 3

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|-------|---|--|---|--|--|---|--|--|--|--|--|--|---|---|---|
| 10:30 | <b>C2L-01</b><br>RF and mm-Wave Power Amplifiers and Combiner (5 papers)<br>Chr: Luis Oliveira, Raafat Labadibi<br>Track: 1 | <b>C2L-02</b><br>SAR ADC Calibration and Energy Optimization (5 papers)<br>Chr: Edoardo Bonizzoni, Sohmyung Ha<br>Track: 1 | <b>C2L-03</b><br>Advanced Analog and Mixed-Signal Techniques II (5 papers)<br>Chr: Joseph Chang, Vanessa Chen<br>Track: 1 | <b>C2L-04</b><br>Low-Power Logic, Circuits & Architectures I (5 papers)<br>Chr: Yuan Du, Chung-An Shen<br>Track: 2 | <b>C2L-05</b><br>Design and Verification of Digital Integrated Circuits and Systems I (5 papers)<br>Chr: Tian-Sheuan Chang, Meiqi Wang<br>Track: 2 | <b>C2L-06</b><br>CAS Education and Outreach and the Open Silicon Initiative (5 papers)<br>Chr: Ljiljana Trajkovic, Ibrahim Elfadel<br>Track: 13 | <b>C2L-07</b><br>Modeling, Control, and Power Management (5 papers)<br>Chr: Zhen Li, Federico Bizzarri<br>Track: 4 | <b>C2L-08</b><br>WF-IoT (5 papers)<br>Chr: Hui Zhang, Bo Zhao<br>Track: 18 | <b>C2L-09</b><br>Hardware-Aware Neural Networks (5 papers)<br>Chr: Chang Gao, Hui Chen<br>Track: 8 | <b>C2L-10</b><br>Image Processing: Segmentation, Compression, Restoration, Registration, and Enhancement (4 papers)<br>Chr: Qing Shen, Izzet Kale<br>Track: 10 | <b>C2L-11</b><br>Conventional and Emerging Memory Circuits and Architectures (5 papers)<br>Chr: Ettore Napoli, Huidong Zhao<br>Track: 14 | <b>C2L-12</b><br>Video Coding (5 papers)<br>Chr: Li Li, Amritha Premkumar<br>Track: 11 | <b>C2L-13</b><br>Specialized Hardware for Embodied AI Application and Neuromorphic Computing II (5 papers)<br>Chr: Yueting Li, Bo Li<br>Track: 15 | <b>C2L-14</b><br>Flexible Electronics (4 papers)<br>Chr: Mayank Kumar Singh, Tong Ge<br>Track: 18 | <b>Poster Session</b><br>Room: SHICC Lobby, Level 3 |
| 11:00 | Conference Room: 3C, SHICC, Level 3   | Conference Room: 3I+3J, SHICC, Level 3   | Conference Room: 3A, SHICC, Level 3   | Conference Room: 3D, SHICC, Level 3  | Conference Room: 3E, SHICC, Level 3  | Conference Room: 3B, SHICC, Level 3   | Conference Room: 3G, SHICC, Level 3  | Conference Room: 5C, SHICC, Level 5  | Conference Room: 5F, SHICC, Level 5  | Conference Room: 5D, SHICC, Level 5  | Conference Room: 5H, SHICC, Level 5  | Conference Room: 5E, SHICC, Level 5  | Conference Room: 5A, SHICC, Level 5   | Conference Room: 5B, SHICC, Level 5   |   |
| 11:30 |   |  |   |  |  |   |  |  |  |  |  |  |   |   |   |

**Lunch**  
Room: Mandarin Hall, SHICC, Level 1

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| 13:30 | <b>C3L-01</b><br>RF Switches, Couplers, and Phase Control (5 papers)<br>Chr: Xi Zhu, Gaetano Palumbo<br>Track: 1 | <b>C3L-02</b><br>Precision and Low-Noise Amplifiers (5 papers)<br>Chr: Salvatore Pennisi, Jose Martinez<br>Track: 1 | <b>C3L-03</b><br>Modeling Methods for Nonlinear Circuits and Systems I (5 papers)<br>Chr: Erivelton Nepomuceno, Yan Liang<br>Track: 9 | <b>C3L-04</b><br>Low-Power Logic, Circuits & Architectures II (5 papers)<br>Chr: Bruce Sham, Bo Wang<br>Track: 2 | <b>C3L-05</b><br>Design and Verification of Digital Integrated Circuits and Systems II (5 papers)<br>Chr: Chi-Chia Sun, Yun Wu<br>Track: 2 | <b>C3L-06</b><br>Breaking Barriers in Privacy-Preserving Machine Learning: From Algorithms to Accelerators (5 papers)<br>Chr: Yingjie Lao, Danella Zhao<br>Track: 15 | <b>C3L-07</b><br>Bridging Algorithms, Circuits, and Systems: Foundations and Applications of Artificial Intelligence (5 papers)<br>Chr: Kai Xu, Jinbo Chen<br>Track: 15 | <b>C3L-08</b><br>Energy-Efficient & High-Resolution Data Converters for Next-Generation Biomedical & Neural Interface (5 papers)<br>Chr: Yang Zhao, Xinsheng Wang<br>Track: 15 | <b>C3L-09</b><br>Neuromorphic Perception and Control (4 papers)<br>Chr: Zhuo Zou, Xumeng Zhang<br>Track: 8 | <b>C3L-10</b><br>Image Processing: AI in Circuits and Systems (5 papers)<br>Chr: Izzet Kale, Yudong Zhang<br>Track: 10 | <b>C3L-11</b><br>Edge Computing (5 papers)<br>Chr: Xilin Liu, Yuan Zhang<br>Track: 14 | <b>C3L-12</b><br>Learning-based Image/Video Coding (5 papers)<br>Chr: Zhu Li, Huaying Wu<br>Track: 11 | <b>C3L-13</b><br>Analysis and Optimization of Complex Systems and Artificial Intelligence Applications I (4 papers)<br>Chr: Xi Zhang, Jiancheng Zhao<br>Track: 15 | <b>Poster Session</b><br>Room: SHICC Lobby, Level 3 |
| 14:00 | Conference Room: 3C, SHICC, Level 3  | Conference Room: 3I+3J, SHICC, Level 3  | Conference Room: 3A, SHICC, Level 3   | Conference Room: 3D, SHICC, Level 3  | Conference Room: 3E, SHICC, Level 3  | Conference Room: 3B, SHICC, Level 3  | Conference Room: 3G, SHICC, Level 3   | Conference Room: 5C, SHICC, Level 5  | Conference Room: 5F, SHICC, Level 5  | Conference Room: 5D, SHICC, Level 5  | Conference Room: 5H, SHICC, Level 5   | Conference Room: 5E, SHICC, Level 5   | Conference Room: 5A, SHICC, Level 5   |   |
| 14:30 |  |   |   |  |  |  |   |  |  |  |   |   |   |   |

**Coffee Break**  
Room: Exhibition Area & Poster Gallery, SHICC, Level 3

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|-------|--|--|--|--|---|--|--|--|---|---|--|--|---|--|
| 16:00 |  |  | <b>C5L-03</b><br>Advanced Circuits and Systems for High-Speed Data Links and Wireless Connectivity (5 papers)<br>Chr: Li Gao, Pei Qin<br>Track: 15 | <b>C5L-04</b><br>Low-Power Logic, Circuits & Architectures III (5 papers)<br>Chr: Yuan Du, Hongbin Sun<br>Track: 2 | <b>C5L-05</b><br>Circuits and Systems for Physiological Sign Detection and Risk Warning in the Elderly (5 papers)<br>Chr: Eva Guttmann-Flury, Hongming Lyu<br>Track: 15 | <b>C5L-06</b><br>Cross-Layer Innovation in Computer-in-Memory Chips (5 papers)<br>Chr: Haozhe Zhu, Jingjing Liu<br>Track: 15 | <b>C5L-07</b><br>Application-Specific Computer Arithmetic for Post-Quantum Cryptography & Homomorphic Encryption Access (5 papers)<br>Chr: Amir Sabbagh Molahosseini, Zhenglai Wang<br>Track: 15 | <b>C5L-08</b><br>Integrated Circuits and Systems for Intelligent Edge and Biomedical Applications (4 papers)<br>Chr: Hong Zhang, Qinyu Chen<br>Track: 15 | <b>C5L-09</b><br>Quantization, Approximation, and Compression for ML Hardware II (5 papers)<br>Chr: Joseph Schmitz, Biao Sun<br>Track: 14 | <b>C5L-10</b><br>Compressive Sensing and Sparse Signal Processing (5 papers)<br>Chr: Deruo Cheng, Wing-Kuen Ling<br>Track: 10 | <b>C5L-11</b><br>Cross-Layer Optimization for Machine Learning (5 papers)<br>Chr: Ibrahim Elfadel<br>Track: 14 | <b>C5L-12</b><br>Volumetric video coding and communication (5 papers)<br>Chr: Lu Yu, Zhengxue Cheng<br>Track: 11 | <b>C5L-13</b><br>Analysis and Optimization of Complex Systems and Artificial Intelligence Applications II (5 papers)<br>Chr: Xi Zhang, Wei Mao<br>Track: 15 |  |
| 16:30 |  |  | Conference Room: 3A, SHICC, Level 3  | Conference Room: 3D, SHICC, Level 3  | Conference Room: 3E, SHICC, Level 3   | Conference Room: 3B, SHICC, Level 3  | Conference Room: 3G, SHICC, Level 3  | Conference Room: 5C, SHICC, Level 5  | Conference Room: 5F, SHICC, Level 5   | Conference Room: 5D, SHICC, Level 5   | Conference Room: 5H, SHICC, Level 5  | Conference Room: 5E, SHICC, Level 5  | Conference Room: 5A, SHICC, Level 5   |  |
| 17:00 |  |  |  |  |   |  |  |  |   |   |  |  |   |  |

**Farewell Reception: Huangpu River Cruise**  
17:40 Group Departure from Venue (10-min walk)  
18:30 Cruise Departure  
Location: Oriental Pearl Tourism Wharf

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| 18:00 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 20:30 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |