ISCAS 2026

IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS

2026 IEEE International Symposium on Circuits and Systems

Circuits and Systems for Intelligent Society

Time: May 24-27,2026

Venue: Shanghai, China

PROGRAM

CONTENTS

General Chairs Welcome Message 1
TPC Welcome Message 3
ISCAS 2026 Organizing Committee 5
Program at a Glance 8
General Information 8
Conference Venue Map 13
IEEE Circuits and Systems Society 15
Circuits and Systems Society Editors 16
IEEE Gustav Robert Kirchhoff Award 16
Conference Sponsors & Exhibitors 17
Social Events Guide 18
Keynote Speakers 19
Tutorial 24
Workshop Session 41
WiCAS-YPCAS Event 58
Industry Forum I 61
Industry Forum II 64
IEEE CASS Student Design Competition 65
IEEE CASS Mentoring Program 66
Lecture Presentations (Oral) 68
Lecture Session Schedule - Detailed Agenda 69
Poster Session Assignments & Guidelines 130
Poster Session Schedule- Detailed Agenda 133
Live Demo Assignments & Guidelines 172
Live Demo Session Schedule- Detailed Agenda 174
ISCAS 2027 Announcement 177

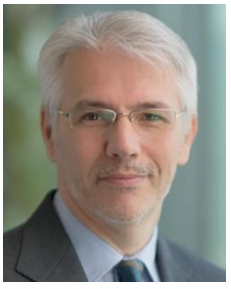
General Chairs Welcome Message

Junfa Mao
Honorary Chair
Shenzhen University,
China

Yong Lian
General Co-Chair
York University,
Canada

Ming Liu
General Co-Chair
Fudan University,
China

Shaojun Wei
General Co-Chair
Tsinghua University,
China



Gianluca Setti
General Co-Chair
King Abdullah University
of Science and
Technology,
Saudi Arabia

On behalf of the Organizing Committee, it is our great pleasure to welcome you to the 2026 IEEE International Symposium on Circuits and Systems (ISCAS 2026), held in Shanghai, China, from May 24 to 27, 2026.

ISCAS is the flagship conference of the IEEE Circuits and Systems Society, and this year's symposium continues its tradition of excellence by bringing together researchers, practitioners, and industry leaders from around the world. Under the theme **"Circuits and Systems for Intelligent Society"**, ISCAS 2026 aims to catalyze transformative innovation at the intersection of circuits, systems, and artificial intelligence, fostering the development of a smart and sustainable society.

We are proud to present a rich and diverse technical program. The symposium features five distinguished keynote talks delivered by globally renowned experts from academia and industry, addressing cutting-edge topics ranging from semiconductor innovation and quantum technologies to energy-efficient computing and advanced AI architectures. These plenary presentations set the stage for a forward-looking exploration of emerging challenges

and opportunities in our field. The technical program includes over a thousand high-quality papers selected through a rigorous review process, spanning 14 regular tracks as well as special sessions, cross-disciplinary sessions, and live demonstrations. Contributions come from researchers across 50 countries, reflecting the truly global nature of the ISCAS community and reinforcing its role as a premier forum for knowledge exchange and collaboration.

In addition to the core technical program, ISCAS 2026 introduces several special features designed to enrich the overall conference experience. All registered participants will have access to complimentary tutorials, offering valuable learning opportunities across a broad range of emerging topics. The symposium also hosts two satellite workshops, *"Standards for AI, Chiplet, and Healthcare"* and *"Connecting Academia and Industry"*, both aimed at fostering meaningful dialogue among researchers, industry practitioners, and standardization communities. Furthermore, three workshops on Monday and Tuesday afternoon will highlight recent advances and future directions in artificial intelligence and design methodologies for circuits and systems. These sessions will also offer valuable opportunities for direct engagement with industry leaders, emphasizing practical challenges and showcasing cutting-edge innovations in the field.

Beyond the technical program, ISCAS 2026 offers a vibrant social program designed to foster networking and community engagement. Highlights include the Welcome Reception on Sunday evening, the Women in Circuits and Systems (WiCAS) and Young Professionals (YP) event on Monday evening, the Gala Banquet on Tuesday evening, and a Farewell Party on the final day. These gatherings provide excellent opportunities to connect with colleagues, establish new collaborations, and celebrate the achievements of the CAS community.

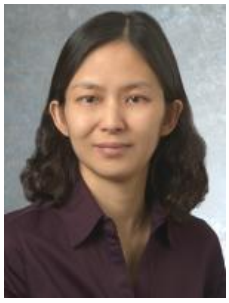
We would like to express our deepest gratitude to the Technical Program Chairs, organizing committee members, track chairs, reviewers, authors, and all volunteers whose dedication and hard work have made this outstanding program possible. We extend special thanks to our student volunteers and sponsors, whose contributions have been invaluable in making this event a success. Their collective efforts ensure that ISCAS continues to uphold its high standards of quality and impact.

We warmly welcome you to Shanghai, a dynamic global city where tradition meets innovation. We hope you will enjoy not only the stimulating technical program, but also the engaging social activities and the vibrant culture and hospitality of the host city.

We wish you a productive, inspiring, and memorable experience at ISCAS 2026.

TPC Welcome Message

Wei-Sheng Zhao
TPC Co-Chair
Beihang University, China



Xinmiao Zhang
TPC Co-Chair
Ohio State University, USA

Eduard Alarcon
TPC Co-Chair
UPC Barcelona Tech, Spain

Yoshifumi Nishio
TPC Co-Chair
Tokushima University, Japan

On behalf of the Technical Program Committee of the 2026 IEEE International Symposium on Circuits and Systems (ISCAS) in Shanghai, it is a genuine pleasure and an honor to welcome you to the technical program of the symposium.

The central technical events within the ISCAS this year will be five keynote talks. We are privileged and grateful to have outstanding presentations by renowned experts: (1) Tingbo He, President of Huawei Semiconductor, will present “New Semiconductor Path in Practice”, (2) M. Jamal Deen, from McMaster University, Canada, will lecture on “Unprecedented Vision - From Single photon Detectors and Pixels to Engineering and Health Systems”, (3) Jian-Wei Pan, from USTC, China, will lecture on “Quantum Network: quantum communication, computation, and metrology”, (4) Giovanni De Micheli, at EPFL, Switzerland, will address “Taming the Dragon: Circuits and Systems for Energy-Efficient and Secure Computation”, and (5) Howard C. Yang, from Montage Technology, China, will present “From Memory-Constrained to Memory-Optimized: How Engram Conditional Memory + MRDIMM/CXL Reshapes Sparse AI Architectures”. We acknowledge Plenary co-chairs, Zhihua Wang, Tsinghua University, China, Mohamad Sawan, Westlake University, China and David Allstot, Carnegie Mellon University, USA, for their leadership.

The ISCAS 2026 Technical Program, driven by an overarching theme of “Circuits and Systems for Intelligent Society”, highlights circuits and systems contributions related to several cross-cutting, multidisciplinary innovation themes, including but not limited to circuits and systems for 6G communication, quantum computing, AI in circuits & systems, security and trust in circuits & systems, and circuits and systems for medicine and healthcare.

From a total of 1673 papers submitted to the 14 regular technical tracks (plus live-demos, special sessions, and cross-society special sessions, with an overall number of 1858 ISCAS paper submissions), the resulting acceptance rate for regular papers was 51.9%, which is in line with the ISCAS tradition of quality, with 869 regular papers accepted in the final technical program of 1009 papers. The program is spread over 122 lecture sessions

and 72 poster sessions.

Papers that made it to the final program originate from 50 different countries, making ISCAS one of the leading opportunities for interaction among the most influential researchers and engineers in the areas of electronic circuits and systems from all over the world.

We have counted on the dedicated effort of 44 Track Chairs, 381 Review Committee Members (RCMs), and 2344 Reviewers. This three-tier articulated review team has allowed us to retrieve 7747 reviews for the papers sent to regular tracks and special sessions, which makes an average of above 4.2 reviews per paper. We are deeply thankful to all of them.

ISCAS 2026 has tightened the collaboration with several CASS flagship Journals, with the main goal of giving authors of high-quality selected ISCAS 2026 papers the possibility to publish a corresponding journal manuscript in a short timeframe.

We want to recognize the Special Sessions Co-Chairs, Yajun Ha, Shanghai Tech University, China, Malgorzata Chrzanowska-Jeske, Portland State University, USA, and especially Elena Blokhina, University College Dublin, Ireland, who put special effort in soliciting proposals and selecting a set of independent RCMs for the review process. Many thanks also to all the special session organizers that helped to put together a cutting-edge program.

Finally, we are also thankful to the Live-Demo Co-Chairs, Peiling Liu, Shanghai Jiao Tong University, China, Xilin Liu, University of Toronto, Canada and especially Philipp Hafliger, University of Oslo, Norway, for leading the selection of a rich set of demonstrators and experimental setups that highlight the innovative character of CAS Community.

We want to recognize Tom Wehner, from epapers, for his diligence and dedication throughout the entire process of building the ISCAS technical program.

We are convinced that IEEE ISCAS 2026 technical program will provide a thriving technical environment to present results and exchange scientific thoughts and visions with colleagues and new peers. We do sincerely hope that you find this Technical Program valuable.

ISCAS 2026 Organizing Committee

Honorary Chair

- **Junfa Mao – Shenzhen University, China**

General Co-Chairs

- **Yong Lian – York University, Canada**
- **Ming Liu – Fudan University, China**
- **Shaojun Wei – Tsinghua University, China**
- **Gianluca Setti – King Abdullah University of Science and Technology, Saudi Arabia**

TPC Co-Chairs

- **Weisheng Zhao – Beihang University, China**
- **Xinmiao Zhang – The Ohio State University, USA**
- **Eduard Alarcón – UPC Barcelona Tech, Spain**
- **Yoshifumi Nishio – Tokushima University, Japan**

Plenary Co-Chairs

- **Zhihua Wang – Tsinghua University, China**
- **Mohamad Sawan – Westlake University, China**
- **David Allstot – Carnegie Mellon University, USA**

Finance Co-Chairs

- **Jian Zhao – Shanghai Jiao Tong University, China**
- **Di He – Shanghai Jiao Tong University, China**

Special Session Co-Chairs

- **Yajun Ha – Shanghai Tech University, China**
- **Elena Blokhina – University College Dublin, Ireland**
- **Malgorzata Chrzanowska-Jeske – Portland State University, USA**

Tutorial Co-Chairs

- **Li Li – University Science and Technology of China, China**
- **Yang Zhao – Shanghai Jiao Tong University, China**

- **Patricia Desgreys – Telecom Paris, France**
- **Shahriar Mirabbasi – University of British Columbia, Canada**

Cross Society Session Co-Chairs

- **Yongfu Li – Shanghai Jiao Tong University, China**
- **Xiaojun Guo – Shanghai Jiao Tong University, China**
- **Shouyi Yin – Tsinghua University, China**
- **Qing Luo – CAS Institute of Microelectronics, China**

Demo Co-Chairs

- **Peiling Liu – Shanghai Jiao Tong University, China**
- **Philipp Hafliger – University of Oslo, Norway**
- **Xilin Liu – University of Toronto, Canada**

WiCAS and YPCAS Co-Chair

- **Julia Chung – National Cheng Kung University**
- **Yoko Uwate – Tokushima University, Japan**
- **Ying Wei – Shandong University, China**

Industry Advisory and Entrepreneurship Co-Chairs

- **Howard Yang – Montage Technology, China**
- **Yu Wang – Tsinghua University, China**
- **Yen-Kuang Chen – Intel, USA**
- **Jie Chen – Fudan University, China**

Publication Co-Chairs

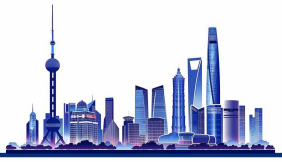
- **Li Geng – Xi'an Jiao Tong University, China**
- **Jianjun Zhou – Shanghai Jiao Tong University, China**
- **Wei Mao – Xidian University, China**

Web Master

- **Xiangting Li – Shanghai Jiao Tong University, China**

Publicity Co-Chairs

- **Boxiao Liu – East China Normal University, China**



- Le Ye – Peking University, China
- Leibo Liu – Tsinghua University, China
- Huaqiang Wu – Tsinghua University, China
- Yongpan Liu – Tsinghua University, China
- Xiaokang Yang – Shanghai Jiao Tong University, China
- Jun Zhou – University of Electronic Science and Technology of China, China
- Zhongfeng Wang – Sun Yat-Sen University, China
- Zhangming Zhu – Xidian University, China
- Gengquan Han – Xidian University, China
- Jun Yang – Southeast University, China
- Xiaoyang Zeng – Fudan University, China

Exhibits Co-Chairs

- Jing Jin – Shanghai Jiao Tong University, China
- Yongxin Zhu – CAS Shanghai Advanced Research Institute, China

Local Arrangement Co-Chairs

- Yan Liu – Shanghai Jiao Tong University, China
- Liang Qi – Shanghai Jiao Tong University, China

International Liaison

- Myung Hoon Sunwoo – Ajou University, South Korea
- An-Yeu (Andy) Wu – National Taiwan University
- Amara Amara – Beihang University, China
- Kea-Tiong (Samuel) Tang – National Tsing Hua University
- Fakhrul Zaman Rokhani – Universiti Putra Malaysia, Malaysia
- Francois Rivet – Bordeaux Institute of Technology, France
- Keshab K. Parhi – University of Minnesota, USA
- Jennifer Blain Christen – Arizona State University, USA
- Carlos Silva-Cardenas – Universitat Autònoma de Barcelona, Spain
- Jose M. de la Rosa – Instituto de Microelectrónica de Sevilla, Spain
- Edoardo Bonizzoni – University of Pavia, Italy
- Shan Liu – Tencent America, USA
- Pedram Mohseni – Case Western Reserve University, USA
- Nicole McFarlane – University of Tennessee, USA
- Yiran Chen – Duke University, USA

Program at a Glance

The symposium follows a structured four-day schedule designed for maximum academic and professional exchange:

- **Sunday (May 24):** Full-day Tutorials and Workshops focusing on emerging research topics. The day concludes with the Welcome Reception in the evening, providing the first opportunity for networking.
- **Monday to Wednesday (May 25–27):** The main conference program featuring 5 high-profile Keynote Speeches, parallel technical sessions (Oral and Poster), and Industrial Forums.
- **Social Highlight: The Gala Dinner and Awards Ceremony will be held on Tuesday (May 26) evening, celebrating excellence in the CAS community and offering unparalleled networking opportunities with global leaders.**

General Information

Venue: Shanghai International Convention Center (SHICC), a landmark overlooking the Bund.

Registration & Badge Collection: The registration desk is located in the 1F Lobby, accessible through Gate 1 of the Shanghai International Convention Center.

- **May 24 (Sunday):** 10:00 – 22:00
- **May 25 – 27 (Monday – Wednesday):** 08:00 – 18:00

Transportation:

- **By Taxi / Driving:**
  - From Pudong International Airport (PVG): Approx. 43 km | 50 minutes.
  - From Hongqiao Airport (SHA): Approx. 20 km | 30 minutes.
  - From Shanghai Railway Station: Approx. 8.4 km | 30 minutes.
- **By Metro:** Take Metro Line 2 or Line 14 to Lujiazui Station. Leave from Exit 2 and walk approximately 700 meters to reach the venue.

Session Protocol: All sessions will start promptly according to the schedule. Speakers are required to check-in at their respective session rooms at least 15 minutes before the session begins.

Publication: All presented papers will be submitted for inclusion in IEEE Xplore, subject to meeting IEEE Xplore's scope and quality requirements.

Weather: Shanghai enters early summer in late May. Temperatures typically range from 18°C to 26°C. As it is the pre-monsoon season, we recommend carrying a folding umbrella.

Digital Readiness in Shanghai: To enjoy a seamless trip, we highly recommend downloading Alipay and linking your international credit card before arrival. For internet access, international roaming is suggested for direct access to global services.

Electricity: The standard voltage in China is 220V. Power outlets are typically Type A, C, and I. We recommend bringing a universal travel adapter.

ISCAS 2026
IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS

Program at a Glance

SUNDAY, MAY 24, 2026

08:00	**Registration (8:00 AM–18:00 PM)** Convention Center Lobby, SHICC, Level 1									
08:30	**T1 - From Circuits to Startups: Translating Innovation into Impact (Entrepreneurship Tutorial)** Conference Room: 5B+5C, SHICC, Level 5	**T2 - AI-Enhanced Implementation of High-Efficiency Delta-Sigma ADCs** Conference Room: 5H, SHICC, Level 5	**T5 - CoDeCAS: Co-designing Devices, Circuits, Systems and Algorithms for Uncertainty aware Multimodal Artificial Intelligence at the Edge** Conference Room: Yangtze River Hall, SHICC, Level 5	**T6 - Power electronic circuits-based safety enhancement techniques for lithium-ion batteries** Conference Room: 5F, SHICC, Level 5	**T7 - High-Throughput Neural Signal Acquisition: Hardware Implementation and Bio-Inspired Approaches** Conference Room: 5A, SHICC, Level 5	**T8 - Advancing Spatial Intelligence —— Geometric Modeling, Representation Learning, and 3D Compression** Conference Room: 5I, SHICC, Level 5	**T9 - From SNNs to Silicon: Automated hardware deployment of spiking neural networks** Conference Room: 5D+5E, SHICC, Level 5	**T16 - Mm-Wave to THz Signal Generation in CMOS: An Injection Locking Approach** Conference Room: 5J, SHICC, Level 5	**Standard Workshop** Conference Room: 3A, SHICC, Level 3		**Workshop of the Cryo-Electronics for Quantum Systems and HPC (Cryo4QHPC) Special Interest Group** Conference Room: 3D, SHICC, Level 3
09:00											
09:30											
10:00	**Coffee Break** Room: Convention Center Lobby, SHICC, Level 5										
10:30	**T1 - From Circuits to Startups: Translating Innovation into Impact (Entrepreneurship Tutorial)** Conference Room: 5B+5C, SHICC, Level 5	**T2 - AI-Enhanced Implementation of High-Efficiency Delta-Sigma ADCs** Conference Room: 5H, SHICC, Level 5	**T5 - CoDeCAS: Co-designing Devices, Circuits, Systems and Algorithms for Uncertainty aware Multimodal Artificial Intelligence at the Edge** Conference Room: Yangtze River Hall, SHICC, Level 5	**T6 - Power electronic circuits-based safety enhancement techniques for lithium-ion batteries** Conference Room: 5F, SHICC, Level 5	**T7 - High-Throughput Neural Signal Acquisition: Hardware Implementation and Bio-Inspired Approaches** Conference Room: 5A, SHICC, Level 5	**T8 - Advancing Spatial Intelligence —— Geometric Modeling, Representation Learning, and 3D Compression** Conference Room: 5I, SHICC, Level 5	**T9 - From SNNs to Silicon: Automated hardware deployment of spiking neural networks** Conference Room: 5D+5E, SHICC, Level 5	**T16 - Mm-Wave to THz Signal Generation in CMOS: An Injection Locking Approach** Conference Room: 5J, SHICC, Level 5	**Standard Workshop** Conference Room: 3A, SHICC, Level 3		
11:00											
11:30											
12:00	**Lunch**										
12:30											
13:00											
13:30	**T17 - Efficient Learning-based Models for Multimodal Data Compression** Conference Room: 5B+5C, SHICC, Level 5	**T13 - Optical Biotelemetry Systems: Basics and Advances for Wireless Data and Power Transmission in Biomedical Implants** Conference Room: 5H, SHICC, Level 5	**T11 - Visual Signal Processing from Human to Embodied Intelligence** Conference Room: Yangtze River Hall, SHICC, Level 5	**T4 - Towards 6G UWB Signal Processing Chain Design** Conference Room: 5F, SHICC, Level 5	**T15 - Modern Power Amplifier Design: From Classical Principles to AI-Assisted Optimization** Conference Room: 5A, SHICC, Level 5	**T12 - Intelligent Design of Wireless Power Transfer: From Fundamentals to AI-Driven Frameworks** Conference Room: 5I, SHICC, Level 5	**T10 - Low-voltage frequency generation, modulation, and demodulation circuits for mobile IoT** Conference Room: 5D+5E, SHICC, Level 5	**T14 - Leveraging IEEE DataPort and IEEE Data Descriptions for Enhanced Research Impact and Student Engagement** Conference Room: 5J, SHICC, Level 5	**Standard Workshop** Conference Room: 3A, SHICC, Level 3	**CASS-CONNECT: Connecting Academia and Industry Workshop** Conference Room: 3B, SHICC, Level 3	
14:00											**Workshop of the Cryo-Electronics for Quantum Systems and HPC (Cryo4QHPC) Special Interest Group** Conference Room: 3D, SHICC, Level 3
14:30											
15:00	**Coffee Break** Room: Convention Center Lobby, SHICC, Level 5										
15:30	**T17 - Efficient Learning-based Models for Multimodal Data Compression** Conference Room: 5B+5C, SHICC, Level 5	**T13 - Optical Biotelemetry Systems: Basics and Advances for Wireless Data and Power Transmission in Biomedical Implants** Conference Room: 5H, SHICC, Level 5	**T11 - Visual Signal Processing from Human to Embodied Intelligence** Conference Room: Yangtze River Hall, SHICC, Level 5	**T4 - Towards 6G UWB Signal Processing Chain Design** Conference Room: 5F, SHICC, Level 5	**T15 - Modern Power Amplifier Design: From Classical Principles to AI-Assisted Optimization** Conference Room: 5A, SHICC, Level 5	**T12 - Intelligent Design of Wireless Power Transfer: From Fundamentals to AI-Driven Frameworks** Conference Room: 5I, SHICC, Level 5	**T10 - Low-voltage frequency generation, modulation, and demodulation circuits for mobile IoT** Conference Room: 5D+5E, SHICC, Level 5	**T14 - Leveraging IEEE DataPort and IEEE Data Descriptions for Enhanced Research Impact and Student Engagement** Conference Room: 5J, SHICC, Level 5	**Standard Workshop** Conference Room: 3A, SHICC, Level 3		
16:00											
16:30											
17:00											
17:30											
18:00	**Welcome Reception** Room: Pearl Hall & Foyer, Shanghai Min, SHICC, Level 7										
21:00											

[Digital Guide & Services]

Platinum Elite Sponsors

Gold Premium Sponsors

Basic Professional Sponsors

MONDAY, MAY 25, 2026

08:00	**Registration (8:00 AM–18:00 PM)** Room: Convention Center Lobby, SHICC, Level 1																
08:30	**Opening Ceremony** Conference Room: Grand Ballroom 1, SHICC, Level 7																
09:00	**Keynote: New Semiconductor Path in Practice** Conference Room: Grand Ballroom 1, SHICC, Level 7																
09:30																	
10:00	**Coffee Break** Room: Grand Ballroom 1 Foyer, SHICC, Level 7/Exhibition Area & Poster Gallery, SHICC, Level 3													**Poster Session & Live Demo** Room: SHICC Lobby, Level 3			
10:30	**A2L-01** **Modeling, Sensors, and Emerging Analog Systems (5 papers)** **Chr: Yi Zhong, Nagendra Krishnapura** **Track: 1** Conference Room: 3C, SHICC, Level 3	**A2L-02** **High-Speed Data Converters and Time-Domain ADCs (5 papers)** **Chr: Tawfiq Musah, Luis Oliveira** **Track: 1** Conference Room: 3I+3J, SHICC, Level 3	**A2L-03** **High-Speed Interface and Wireline Circuits (5 papers)** **Chr: Navid Yazdi, Yanquan Luo** **Track: 1** Conference Room: 3A, SHICC, Level 3	**A2L-04** **Hardware Security for Internet-of-Things, Cyber-Physical Systems I (5 papers)** **Chr: Preet Yadav, Yeong-Kang Lai** **Track: 2** Conference Room: 3D, SHICC, Level 3	**A2L-05** **SoC, NoC, Multi-Core, and 3D/2.5D Integrated Circuits and Systems I (5 papers)** **Chr: Fakhrul Zaman Rokhani, Danella Zhao** **Track: 2** Conference Room: 3E, SHICC, Level 3	**A2L-06** **Post-Quantum Cryptography and High-Speed Links (5 papers)** **Chr: Dur-e-Shahwar Kundi, Youngjoo Lee** **Track: 3** Conference Room: 3B, SHICC, Level 3	**A2L-07** **Integrated Power Circuits and Charge Pumps (5 papers)** **Chr: Xiaolu Lucia Li, Yang Jiang** **Track: 4** Conference Room: 3G, SHICC, Level 3	**A2L-08** **Ferroelectric and Memristive in-Memory Computing (5 papers)** **Chr: Kyeong-Sik Min, Vasilis Ntinas** **Track: 5** Conference Room: 5C, SHICC, Level 5	**A2L-09** **Spiking Neural Network Architectures and Learning (5 papers)** **Chr: Qinyu Chen, Xiaofang Pan** **Track: 8** Conference Room: 5F, SHICC, Level 5	**A2L-10** **Image and Vision Sensors I (5 papers)** **Chr: Ricardo Carmona Galan, Joseph Schmitz** **Track: 7** Conference Room: 5D, SHICC, Level 5	**A2L-11** **Acellerators for Machine Learning (5 papers)** **Chr: Walter Leon Salas, Weixiong Jiang** **Track: 14** Conference Room: 5H, SHICC, Level 5	**A2L-12** **Representation and Compression for Vision and Multimodal Learning Systems (5 papers)** **Chr: Shiqi Wang, Qingsong Xie** **Track: 12** Conference Room: 5E, SHICC, Level 5	**A2L-13** **Synergies between Emerging AI Technologies and Circuits and Systems (5 papers)** **Chr: Adam Liu, Yue Zhang** **Track: 15** Conference Room: 5A, SHICC, Level 5	**A2L-14** **AI for Medical Signal and Image Analysis (4 papers)** **Chr: Mohamad Sawan, Yunshan Zhang** **Track: 6** Conference Room: 5B, SHICC, Level 5		
11:00																	
11:30																	
12:00	**Lunch** Room: Mandarin Hall, SHICC, Level 1																
12:30																	
13:00																	
13:30	**Keynote: Unprecedented Vision - From Single photon Detectors and Pixels to Engineering and Health Systems** Conference Room: Grand Ballroom 1, SHICC, Level 7																
14:00																	
14:30	**Coffee Break** Room: Exhibition Area & Poster Gallery, SHICC, Level 3													**Poster Session** Room: SHICC Lobby, Level 3			
15:00	**A4L-01** **AI-Assisted and Emerging Analog Circuits (5 papers)** **Chr: Gordon Roberts, Liangjian Lyu** **Track: 1** Conference Room: 3C, SHICC, Level 3	**A4L-02** **Pipeline and Non-Conventional ADC Architectures (5 papers)** **Chr: Jorge Fernandes, Edoardo Bonizzoni** **Track: 1** Conference Room: 3I+3J, SHICC, Level 3	**A4L-03** **Voltage References and Power Management (5 papers)** **Chr: Filippo Neri, Bibhu Sahoo** **Track: 1** Conference Room: 3A, SHICC, Level 3	**A4L-04** **Datapath & Arithmetic Circuits and Systems I (5 papers)** **Chr: Ettore Napoli, Hao Zhang** **Track: 2** Conference Room: 3D, SHICC, Level 3	**A4L-05** **SoC, NoC, Multi-Core, and 3D/2.5D Integrated Circuits and Systems II (5 papers)** **Chr: Huiyun Li, Fakhrul Zaman Rokhani** **Track: 2** Conference Room: 3E, SHICC, Level 3	**A4L-06** **Wireless Communications I (5 papers)** **Chr: Jienan Chen, Shan Cao** **Track: 3** Conference Room: 3B, SHICC, Level 3	**A4L-07** **High Efficiency Converters and Drive Circuits for Specialized Applications (5 papers)** **Chr: Mo Huang, Hui Wang** **Track: 4** Conference Room: 3G, SHICC, Level 3	**A4L-08** **Spintronics-based In-Memory Computing (5 papers)** **Chr: Hongwu Jiang, Vasilis Ntinas** **Track: 5** Conference Room: 5C, SHICC, Level 5	**A4L-09** **Neuromorphic Circuits and Neuron Implementations (5 papers)** **Chr: Jim Harkin, Zhenglai Wang** **Track: 8** Conference Room: 5F, SHICC, Level 5	**A4L-10** **Biochemical and Environmental Sensors (5 papers)** **Chr: Paula Lopez Martinez, Juan Antonio Leñero-Bardallo** **Track: 7** Conference Room: 5D, SHICC, Level 5	**A4L-11** **Circuits, Systems and Architectures for Machine Learning I (5 papers)** **Chr: Ibrahim Elfadel, Weijie Jiang** **Track: 14** Conference Room: 5H, SHICC, Level 5	**A4L-12** **Architectures and Compression Techniques for Rendering, Perception, and Forecasting (5 papers)** **Chr: Li Li, Xin Lou** **Track: 12** Conference Room: 5E, SHICC, Level 5	**A4L-13** **Artificial Intelligence in Power and Energy Circuits and Systems I (5 papers)** **Chr: Herbert Iu, Qing Zhang** **Track: 15** Conference Room: 5A, SHICC, Level 5	**A4L-14** **Bio-Signal Acquisition Front-Ends (5 papers)** **Chr: Hua Fan, Jiangchao Wu** **Track: 6** Conference Room: 5B, SHICC, Level 5	**IEEE CASS Student Design Competition** Conference Room: Yangtze River Hall, SHICC, Level 5	**Artificial Intelligence Workshop: Foundation Models, Compute Platforms, and Emerging Application** Conference Room: 5J, SHICC, Level 5
15:30																**IEEE CASS Mentoring Program** Conference Room: Yangtze River Hall, SHICC, Level 5	
16:00																	
16:30	**A5L-01** **Programmable, High-Drive, and High-Voltage Amplifiers (5 papers)** **Chr: Salvatore Pennisi, Gaetano Palumbo** **Track: 1** Conference Room: 3C, SHICC, Level 3	**A5L-02** **Delta–Sigma ADCs and DAC Techniques (5 papers)** **Chr: Jose de la Rosa, Qiang Li** **Track: 1** Conference Room: 3I+3J, SHICC, Level 3	**A5L-03** **VCO Design and Oscillator Techniques (5 papers)** **Chr: Jorge Fernandes, Lei Zhang** **Track: 1** Conference Room: 3A, SHICC, Level 3	**A5L-04** **Datapath & Arithmetic Circuits and Systems II (5 papers)** **Chr: Hao Zhang, Ettore Napoli** **Track: 2** Conference Room: 3D, SHICC, Level 3	**A5L-05** **Electronic Design Automation and Physical Design I (5 papers)** **Chr: Xinfei Guo, Lan-Da Van** **Track: 2** Conference Room: 3E, SHICC, Level 3	**A5L-06** **Wireless Communications II (5 papers)** **Chr: Shan Cao, Joungsun Park** **Track: 3** Conference Room: 3B, SHICC, Level 3	**A5L-07** **Circuits and Systems for Wireless Power Transfer applications (5 papers)** **Chr: Zhicong Huang, Chi-Seng Lam** **Track: 4** Conference Room: 3G, SHICC, Level 3	**A5L-08** **Quantum Computing I (5 papers)** **Chr: Georgios Ch. Sirakoulis, Vasilis Ntinas** **Track: 5** Conference Room: 5C, SHICC, Level 5	**A5L-09** **Grand Challenge on Neural Network-based Video Coding (4 papers)** **Chr: Li Zhang, Zhipin Deng** **Track: 17** Conference Room: 5F, SHICC, Level 5	**A5L-10** **Sensory Circuits and Systems I (5 papers)** **Chr: Nicola Massari, Ibrahim Elfadel** **Track: 7** Conference Room: 5D, SHICC, Level 5	**A5L-11** **Circuits, Systems and Architectures for Machine Learning II (5 papers)** **Chr: Ricardo Carmona Galan, Biao Pan** **Track: 14** Conference Room: 5H, SHICC, Level 5	**A5L-12** **Multimodal Dialog, Speech Processing, and 3D Representation (4 papers)** **Chr: Xin Jin, Qingsong Xie** **Track: 12** Conference Room: 5E, SHICC, Level 5	**A5L-13** **Artificial Intelligence in Power and Energy Circuits and Systems II (5 papers)** **Chr: Herbert Iu, Miao Meng** **Track: 15** Conference Room: 5A, SHICC, Level 5	**A5L-14** **Medical Computing Hardware and SoCs (5 papers)** **Chr: Jie Chen, Cheng Han** **Track: 6** Conference Room: 5B, SHICC, Level 5		
17:00																	
17:30																	
18:00	**WiCAS-YPCAS Event** Room: Europe Hall, SHICC, Level 5																
21:30																	

TUESDAY, MAY 26, 2026

Registration (8:00 AM~18:00 PM)
Room: Convention Center Lobby, SHICC, Level 1

Kirchhoff and IEEE CASS Awards
Conference Room: Grand Ballroom 1, SHICC, Level 7

Keynote: Quantum Network: Quantum Communication, Computation, and Metrology
Conference Room: Grand Ballroom 1, SHICC, Level 7

Coffee Break
Room: Exhibition Area & Poster Gallery, SHICC, Level 3

B2L-01
RF Frequency Generation and Synthesizers (4 papers)
Chr: Xi Zhu, Arindam Sanyal
Track: 1
Conference Room: 3C, SHICC, Level 3

B2L-02
Time-Interleaved and High-Speed SAR ADCs (5 papers)
Chr: Yi Shen, Hyeon Kim
Track: 1
Conference Room: 3I+3J, SHICC, Level 3

B2L-03
Oscillators, PLLs, and Clock Generation (5 papers)
Chr: Filippo Neri, Degang Chen
Track: 1
Conference Room: 3A, SHICC, Level 3

B2L-04
Hardware Security for Logic, Circuits and Architectures I (5 papers)
Chr: Martinez Alonso Abdel, Jing Tian
Track: 2
Conference Room: 3D, SHICC, Level 3

B2L-05
Electronic Design Automation and Physical Design II (5 papers)
Chr: Bruce Sham, Kun-Chih Chen
Track: 2
Conference Room: 3E, SHICC, Level 3

B2L-06
Wireline Communications I (5 papers)
Chr: Yuan Du, Xinpeng Xing
Track: 3
Conference Room: 3B, SHICC, Level 3

B2L-07
Circuits and Systems for Enhanced DC-DC Switch-mode Power Supplies (5 papers)
Chr: Yang Jiang, Yanzhao Ma
Track: 4
Conference Room: 3G, SHICC, Level 3

B2L-08
AI Circuits and Architectures (5 papers)
Chr: Ronald Tetzlaff, Wai-Chi Fang
Track: 5
Conference R-oom: 5C, SHICC, Level 5

B2L-09
Compute-in-Memory-Based Neural Computing (5 papers)
Chr: Di He, Yuqi Su
Track: 8
Conference Room: 5F, SHICC, Level 5

B2L-10
Sensory Signal Conditioning (5 papers)
Chr: Mario Renteria Pinon, Yan Liu
Track: 7
Conference Room: 5D, SHICC, Level 5

B2L-11
Quantization, Approximation, and Compression for ML Hardware I (5 papers)
Chr: Milin Zhang, Shiwei Liu
Track: 14
Conference Room: 5H, SHICC, Level 5

B2L-12
Multimodal Interfaces and Efficient Architectures for Intelligent Visual Systems (4 papers)
Chr: Weiyao Lin, Lei Qiu
Track: 12
Conference Room: 5E, SHICC, Level 5

B2L-13
Empowering the Evolving Electrical Grid: Circuits & Systems for Greener Generation, Distribution I (5 papers)
Chr: Federico Bizzarri, C. K. Michael Tse
Track: 15
Conference Room: 5A, SHICC, Level 5

B2L-14
Neural Recording and Stimulation ASICs (5 papers)
Chr: Sohmyung Ha, Tim Constandinou
Track: 6
Conference Room: 5B, SHICC, Level 5

Poster Session & Live Demo
Room: SHICC Lobby, Level 3

Lunch
Room: Mandarin Hall, SHICC, Level 1

Keynote: Taming the Dragon: Circuits and Systems for Energy-efficient and Secure Computation
Conference Room: Grand Ballroom 1, SHICC, Level 7

Coffee Break
Room: Exhibition Area & Poster Gallery, SHICC, Level 3

B4L-01
RF and mm-Wave Low-Noise Amplifiers (5 papers)
Chr: Raafat Labadibi, Luis Oliveira
Track: 1
Conference Room: 3C, SHICC, Level 3

B4L-02
Delta–Sigma and Zoom ADCs (5 papers)
Chr: Qiang Li, Jose de la Rosa
Track: 1
Conference Room: 3I+3J, SHICC, Level 3

B4L-03
Multiphase PLLs and Injection-Locked Clocks (5 papers)
Chr: Shahriar Mirabbasi, Robert Sobot
Track: 1
Conference Room: 3A, SHICC, Level 3

B4L-04
Hardware Security for Logic, Circuits and Architectures II (5 papers)
Chr: Martinez Alonso Abdel, Xiaojin Zhao
Track: 2
Conference Room: 3D, SHICC, Level 3

B4L-05
Electronic Design Automation and Physical Design III (5 papers)
Chr: Xinfei Guo, Tony Tae-Hyoung Kim
Track: 2
Conference Room: 3E, SHICC, Level 3

B4L-06
Homomorphic Encryption and Quantum Circuits (5 papers)
Chr: Xinpeng Xing, Hanho Lee
Track: 3
Conference Room: 3B, SHICC, Level 3

B4L-07
Circuits & Systems for Energy Harvesting I (5 papers)
Chr: Junrui Liang, Jinbo Li
Track: 4
Conference Room: 3G, SHICC, Level 3

B4L-08
Nanoelectronic Circuits (5 papers)
Chr: Feng Zhang, Georgios Ch. Sirakoulis
Track: 5
Conference Room: 5C, SHICC, Level 5

B4L-09
Neuromorphic Processor Architecture and System (5 papers)
Chr: Yuncheng Lu, Xinming Shi
Track: 8
Conference Room: 5F, SHICC, Level 5

B4L-10
Machine Learning for Signal Processing (5 papers)
Chr: Yudong Zhang, Xin Lou
Track: 10
Conference Room: 5D, SHICC, Level 5

B4L-11
Compute-in-Memory I (5 papers)
Chr: Peilin Liu, Zhiting Lin
Track: 14
Conference Room: 5H, SHICC, Level 5

B4L-12
Computational Intelligence for Multimedia Understanding (4 papers)
Chr: Maria Trocan, Behçet Uğur Töreyin
Track: 18
Conference Room: 5E, SHICC, Level 5

B4L-13
Empowering the Evolving Electrical Grid: Circuits & Systems for Greener Generation, Distribution II (4 papers)
Chr: Federico Bizzarri, C. K. Michael Tse
Track: 15
Conference Room: 5A, SHICC, Level 5

B4L-14
Sensing Interfaces and SoCs (5 papers)
Chr: Pantelis Georgiou, Changgui Yang
Track: 6
Conference Room: 5B, SHICC, Level 5

Poster Session
Room: SHICC Lobby, Level 3

Industry Forum I: AI-Driven Innovation for the Future Chip Design
Conference Room: Grand Ballroom 1, SHICC, Level 7

Industry Forum II: Charting the Next Era of Semiconductors
Conference Room: Yellow River, SHICC, Level 3

IEEE CASS Chapter Leadership Workshop @ ISCAS 2026 (Shanghai)
Conference Room: 5I, SHICC, Level 5

B5L-01
RF and mm-Wave Transceivers and Receivers (5 papers)
Chr: Jerald Yoo, Arindam Sanyal
Track: 1
Conference Room: 3C, SHICC, Level 3

B5L-02
Noise-Shaping ADCs and DAC Techniques for SAR ADCs (5 papers)
Chr: Jorge Fernandes, Gonçalo Rodrigues
Track: 1
Conference Room: 3I+3J, SHICC, Level 3

B5L-03
Advanced Analog and Mixed-Signal Techniques I (5 papers)
Chr: Randall Geiger, Ankesh Jain
Track: 1
Conference Room: 3A, SHICC, Level 3

B5L-04
Hardware Security for Logic, Circuits and Architectures III (4 papers)
Chr: Xiaojin Zhao, Chi-Chia Sun
Track: 2
Conference Room: 3D, SHICC, Level 3

B5L-05
Programmable, Reconfigurable & Array Architectures I (5 papers)
Chr: Danella Zhao, Chung-An Shen
Track: 2
Conference Room: 3E, SHICC, Level 3

B5L-06
AI/ML for Communication and Signal Processing (4 papers)
Chr: Youngmin Kim, Shan Cao
Track: 3
Conference Room: 3B, SHICC, Level 3

B5L-07
Circuits & Systems for Energy Harvesting II (5 papers)
Chr: Junrui Liang, Xiongchuan Huang
Track: 4
Conference Room: 3G, SHICC, Level 3

B5L-08
Quantum Computing II (5 papers)
Chr: Hao Cai, Feng Zhang
Track: 5
Conference Room: 5C, SHICC, Level 5

B5L-09
Neuromorphic Learning and Plasticity (5 papers)
Chr: Qinyu Chen, Lianbo Wu
Track: 8
Conference Room: 5F, SHICC, Level 5

B5L-10
Signal Processing Theories and Algorithms for Biosignals (4 papers)
Chr: Wei Liu, Weihao Wang
Track: 10
Conference Room: 5D, SHICC, Level 5

B5L-11
Compute-in-Memory II (5 papers)
Chr: Kannaujiya Aryan, Liang Chang
Track: 14
Conference Room: 5H, SHICC, Level 5

B5L-12
Circuits and Systems for Coding and Processing (5 papers)
Chr: Heming Sun, Hui Zhang
Track: 11
Conference Room: 5E, SHICC, Level 5

B5L-13
Specialized Hardware for Embodied AI Application and Neuromorphic Computing I (5 papers)
Chr: Yueting Li, Bo Li
Track: 15
Conference Room: 5A, SHICC, Level 5

B5L-14
Wireless Power and Implantable Systems (5 papers)
Chr: Arindam Basu, Hanjun Jiang
Track: 6
Conference Room: 5B, SHICC, Level 5

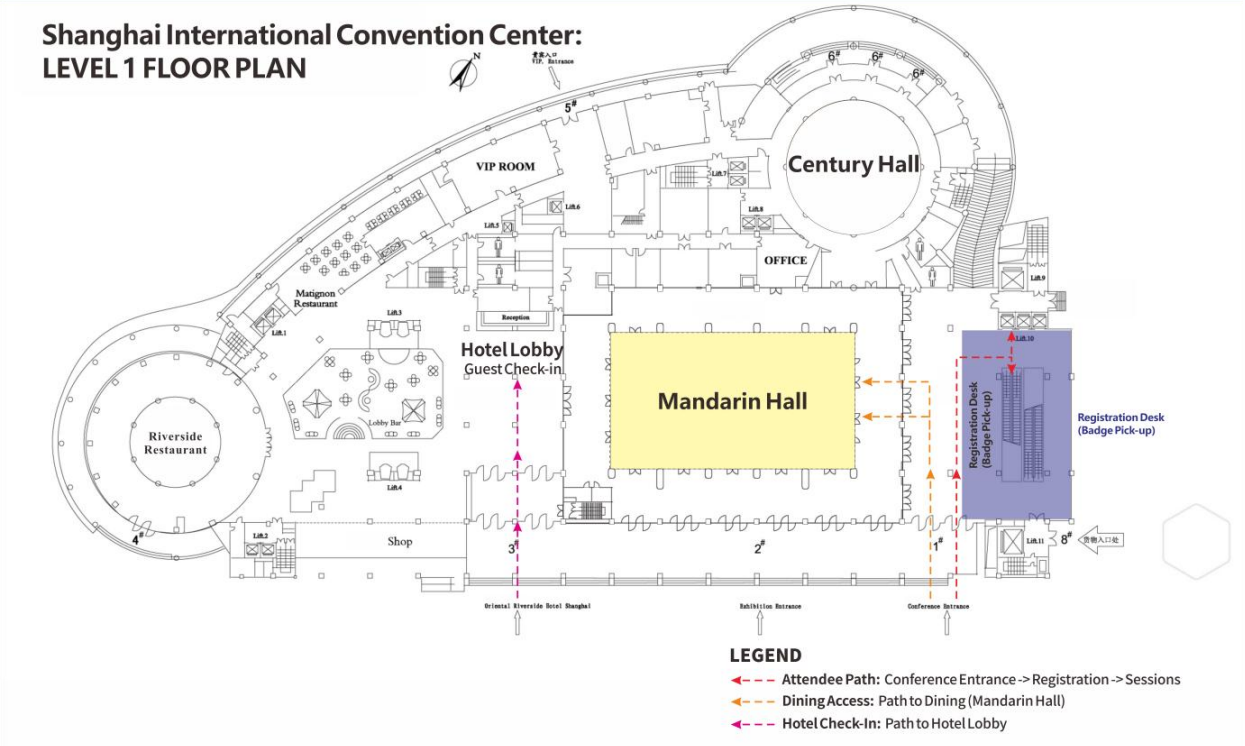
Gala Dinner & ISCAS Awards Ceremony
Conference Room: Grand Ballroom 1, SHICC, Level 7

WEDNESDAY, MAY 27, 2026

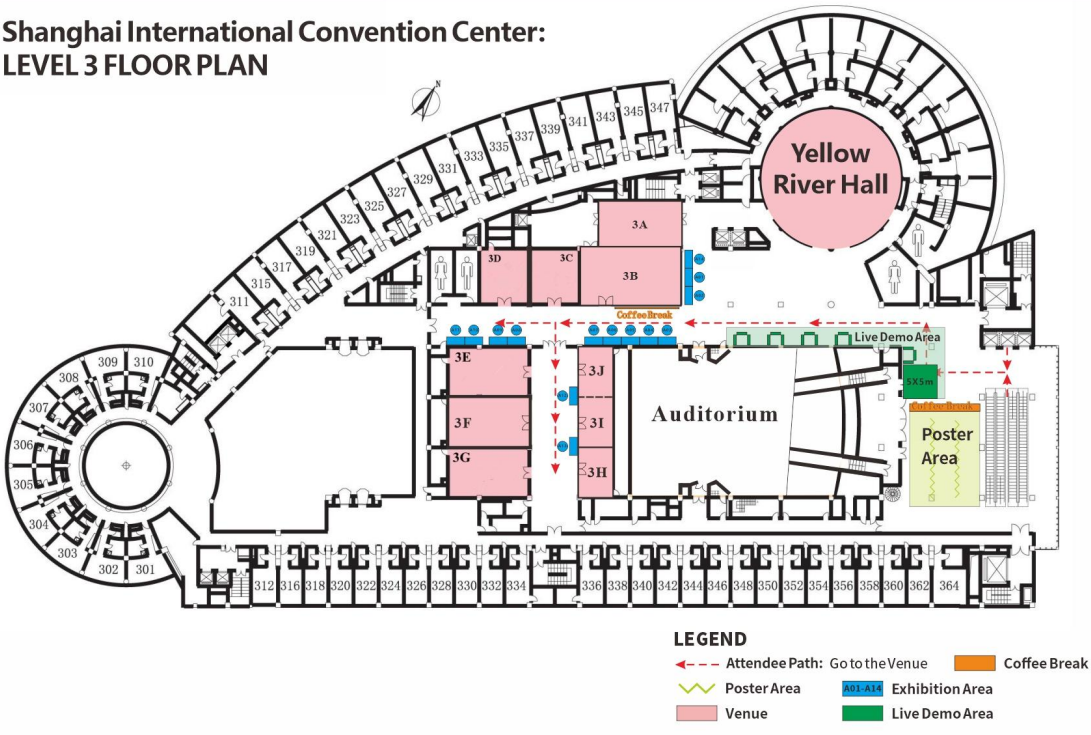
08:30	**Registration (8:30 AM–13:00 PM)** Room: Convention Center Lobby, SHICC, Level 1													
09:00 09:30	**Keynote: From Memory-Constrained to Memory-Optimized: How Engram Conditional Memory + MRDIMM/CXL Reshapes Sparse AI Architectures** Conference Room: Grand Ballroom 1, SHICC, Level 7													
10:00	**Coffee Break** Room: Exhibition Area & Poster Gallery, SHICC, Level 3													**Poster Session** Room: SHICC Lobby, Level 3
10:30 11:00 11:30	**C2L-01** **RF and mm-Wave Power Amplifiers and Combiner (5 papers)** **Chr: Luis Oliveira, Raafat Labadibi** **Track: 1** Conference Room: 3C, SHICC, Level 3	**C2L-02** **SAR ADC Calibration and Energy Optimization (5 papers)** **Chr: Edoardo Bonizzoni, Sohmyung Ha** **Track: 1** Conference Room: 3I+3J, SHICC, Level 3	**C2L-03** **Advanced Analog and Mixed-Signal Techniques II (5 papers)** **Chr: Joseph Chang, Vanessa Chen** **Track: 1** Conference Room: 3A, SHICC, Level 3	**C2L-04** **Low-Power Logic, Circuits & Architectures I (5 papers)** **Chr: Yuan Du, Chung-An Shen** **Track: 2** Conference Room: 3D, SHICC, Level 3	**C2L-05** **Design and Verification of Digital Integrated Circuits and Systems I (5 papers)** **Chr: Tian-Sheuan Chang, Meiqi Wang** **Track: 2** Conference Room: 3E, SHICC, Level 3	**C2L-06** **CAS Education and Outreach and the Open Silicon Initiative (5 papers)** **Chr: Ljiljana Trajkovic, Ibrahim Elfadel** **Track: 13** Conference Room: 3B, SHICC, Level 3	**C2L-07** **Modeling, Control, and Power Management (5 papers)** **Chr: Zhen Li, Federico Bizzarri** **Track: 4** Conference Room: 3G, SHICC, Level 3	**C2L-08** **WF-IoT (5 papers)** **Chr: Hui Zhang, Bo Zhao** **Track: 18** Conference Room: 5C, SHICC, Level 5	**C2L-09** **Hardware-Aware Neural Networks (5 papers)** **Chr: Chang Gao, Hui Chen** **Track: 8** Conference Room: 5F, SHICC, Level 5	**C2L-10** **Image Processing: Segmentation, Compression, Restoration, Registration, and Enhancement (4 papers)** **Chr: Qing Shen, Izzet Kale** **Track: 10** Conference Room: 5D, SHICC, Level 5	**C2L-11** **Conventional and Emerging Memory Circuits and Architectures (5 papers)** **Chr: Ettore Napoli, Huidong Zhao** **Track: 14** Conference Room: 5H, SHICC, Level 5	**C2L-12** **Video Coding (5 papers)** **Chr: Li Li, Amritha Premkumar** **Track: 11** Conference Room: 5E, SHICC, Level 5	**C2L-13** **Specialized Hardware for Embodied AI Application and Neuromorphic Computing II (5 papers)** **Chr: Yueting Li, Bo Li** **Track: 15** Conference Room: 5A, SHICC, Level 5	**C2L-14** **Flexible Electronics (4 papers)** **Chr: Mayank Kumar Singh, Tong Ge** **Track: 18** Conference Room: 5B, SHICC, Level 5	
12:00 12:30 13:00	**Lunch** Room: Mandarin Hall, SHICC, Level 1													
13:30 14:00 14:30	**C3L-01** **RF Switches, Couplers, and Phase Control (5 papers)** **Chr: Xi Zhu, Gaetano Palumbo** **Track: 1** Conference Room: 3C, SHICC, Level 3	**C3L-02** **Precision and Low-Noise Amplifiers (5 papers)** **Chr: Salvatore Pennisi, Jose Martinez** **Track: 1** Conference Room: 3I+3J, SHICC, Level 3	**C3L-03** **Modeling Methods for Nonlinear Circuits and Systems I (5 papers)** **Chr: Erivelton Nepomuceno, Yan Liang** **Track: 9** Conference Room: 3A, SHICC, Level 3	**C3L-04** **Low-Power Logic, Circuits & Architectures II (5 papers)** **Chr: Bruce Sham, Bo Wang** **Track: 2** Conference Room: 3D, SHICC, Level 3	**C3L-05** **Design and Verification of Digital Integrated Circuits and Systems II (5 papers)** **Chr: Chi-Chia Sun, Yun Wu** **Track: 2** Conference Room: 3E, SHICC, Level 3	**C3L-06** **Breaking Barriers in Privacy-Preserving Machine Learning: From Algorithms to Accelerators (5 papers)** **Chr: Yingjie Lao, Danella Zhao** **Track: 15** Conference Room: 3B, SHICC, Level 3	**C3L-07** **Bridging Algorithms, Circuits, and Systems: Foundations and Applications of Artificial Intelligence (5 papers)** **Chr: Kai Xu, Jinbo Chen** **Track: 15** Conference Room: 3G, SHICC, Level 3	**C3L-08** **Energy-Efficient & High-Resolution Data Converters for Next-Generation Biomedical & Neural Interface (5 papers)** **Chr: Yang Zhao, Xinsheng Wang** **Track: 15** Conference Room: 5C, SHICC, Level 5	**C3L-09** **Neuromorphic Perception and Control (4 papers)** **Chr: Zhuo Zou, Xumeng Zhang** **Track: 8** Conference Room: 5F, SHICC, Level 5	**C3L-10** **Image Processing: AI in Circuits and Systems (5 papers)** **Chr: Izzet Kale, Yudong Zhang** **Track: 10** Conference Room: 5D, SHICC, Level 5	**C3L-11** **Edge Computing (5 papers)** **Chr: Xilin Liu, Yuan Zhang** **Track: 14** Conference Room: 5H, SHICC, Level 5	**C3L-12** **Learning-based Image/Video Coding (5 papers)** **Chr: Zhu Li, Huaying Wu** **Track: 11** Conference Room: 5E, SHICC, Level 5	**C3L-13** **Analysis and Optimization of Complex Systems and Artificial Intelligence Applications I (4 papers)** **Chr: Xi Zhang, Jiancheng Zhao** **Track: 15** Conference Room: 5A, SHICC, Level 5		
15:00	**Coffee Break** Room: Exhibition Area & Poster Gallery, SHICC, Level 3													**Poster Session** Room: SHICC Lobby, Level 3
16:00 16:30 17:00			**C5L-03** **Advanced Circuits and Systems for High-Speed Data Links and Wireless Connectivity (5 papers)** **Chr: Li Gao, Pei Qin** **Track: 15** Conference Room: 3A, SHICC, Level 3	**C5L-04** **Low-Power Logic, Circuits & Architectures III (5 papers)** **Chr: Yuan Du, Hongbin Sun** **Track: 2** Conference Room: 3D, SHICC, Level 3	**C5L-05** **Circuits and Systems for Physiological Sign Detection and Risk Warning in the Elderly (5 papers)** **Chr: Eva Guttmann-Flury, Hongming Lyu** **Track: 15** Conference Room: 3E, SHICC, Level 3	**C5L-06** **Cross-Layer Innovation in Computer-in-Memory Chips (5 papers)** **Chr: Haozhe Zhu, Jingjing Liu** **Track: 15** Conference Room: 3B, SHICC, Level 3	**C5L-07** **Application-Specific Computer Arithmetic for Post-Quantum Cryptography & Homomorphic Encryption Access (5 papers)** **Chr: Amir Sabbagh Molahosseini, Zhenglai Wang** **Track: 15** Conference Room: 3G, SHICC, Level 3	**C5L-08** **Integrated Circuits and Systems for Intelligent Edge and Biomedical Applications (4 papers)** **Chr: Hong Zhang, Qinyu Chen** **Track: 15** Conference Room: 5C, SHICC, Level 5	**C5L-09** **Quantization, Approximation, and Compression for ML Hardware II (5 papers)** **Chr: Joseph Schmitz, Biao Sun** **Track: 14** Conference Room: 5F, SHICC, Level 5	**C5L-10** **Compressive Sensing and Sparse Signal Processing (5 papers)** **Chr: Deruo Cheng, Wing-Kuen Ling** **Track: 10** Conference Room: 5D, SHICC, Level 5	**C5L-11** **Cross-Layer Optimization for Machine Learning (5 papers)** **Chr: Ibrahim Elfadel** **Track: 14** Conference Room: 5H, SHICC, Level 5	**C5L-12** **Volumetric video coding and communication (5 papers)** **Chr: Lu Yu, Zhengxue Cheng** **Track: 11** Conference Room: 5E, SHICC, Level 5	**C5L-13** **Analysis and Optimization of Complex Systems and Artificial Intelligence Applications II (5 papers)** **Chr: Xi Zhang, Wei Mao** **Track: 15** Conference Room: 5A, SHICC, Level 5		
17:30														
18:00 20:30	**Farewell Reception: Huangpu River Cruise** **17:40 Group Departure from Venue (10-min walk)** **18:30 Cruise Departure** Location: Oriental Pearl Tourism Wharf													

Conference Venue Map

ISCAS 2026: CONFERENCE VENUE GUIDE

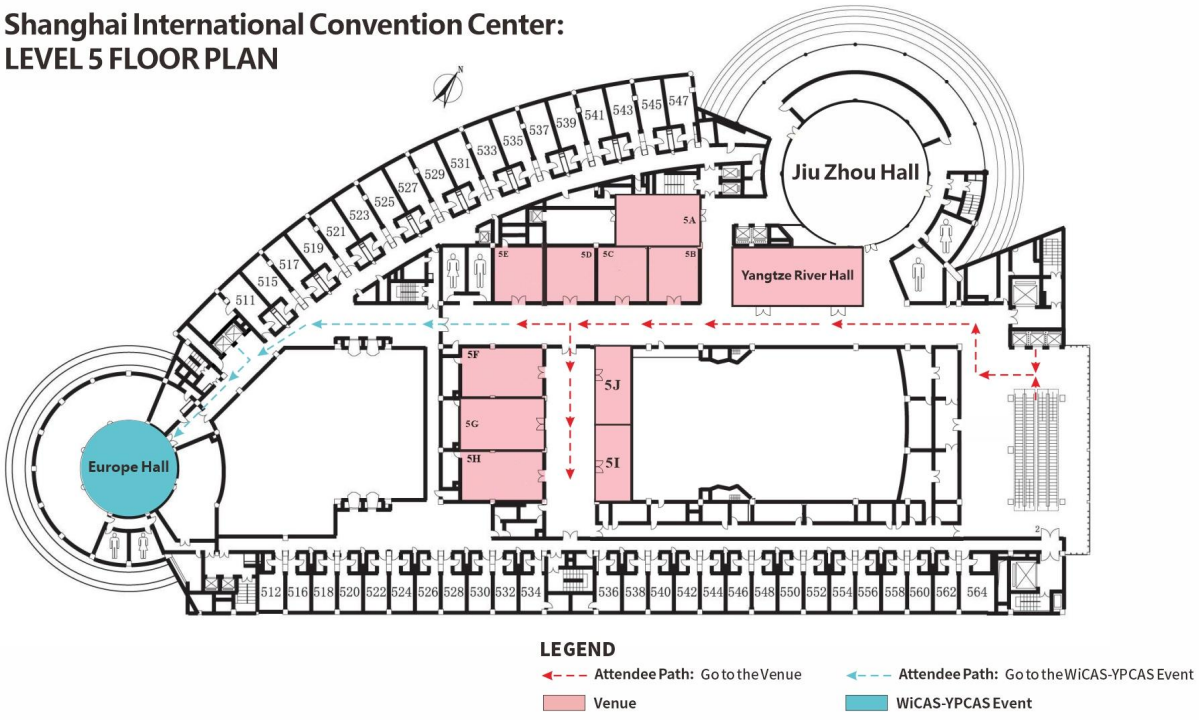


ISCAS 2026: CONFERENCE VENUE GUIDE



ISCAS 2026: CONFERENCE VENUE GUIDE

Shanghai International Convention Center: LEVEL 5 FLOOR PLAN

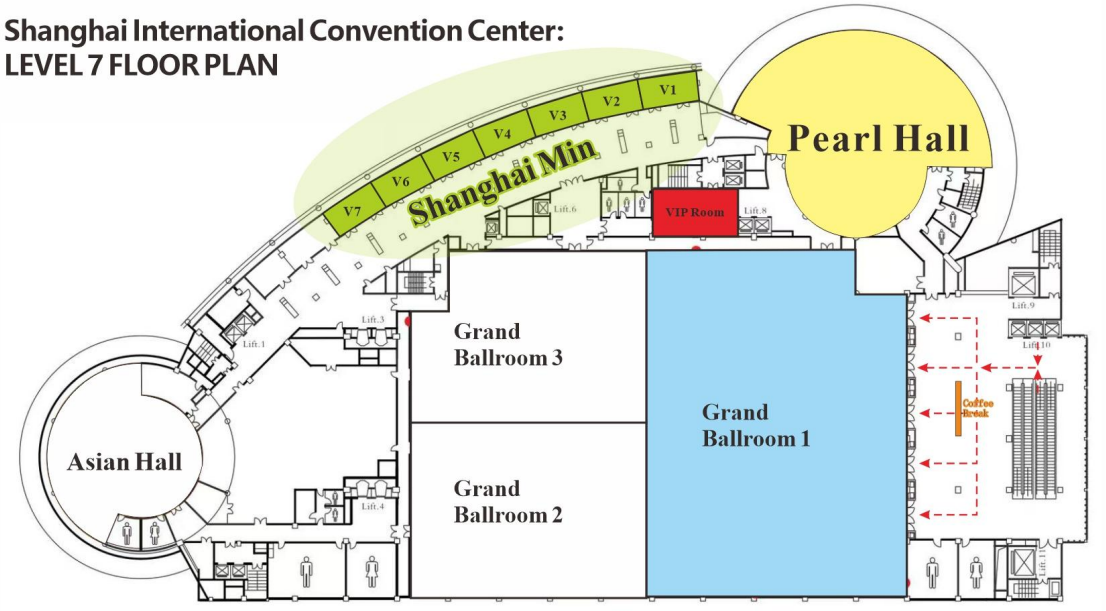


LEGEND

- Attendee Path: Go to the Venue
- Attendee Path: Go to the WiCAS-YPCAS Event
- Venue
- WiCAS-YPCAS Event

ISCAS 2026: CONFERENCE VENUE GUIDE

Shanghai International Convention Center: LEVEL 7 FLOOR PLAN



LEGEND

- Attendee Path: Go to the Main Conference Hall
- Welcome Reception
- Main Conference Hall
- Shanghai Min
- Coffee Break
- VIP Room

IEEE Circuits and Systems Society

Executive Officers

- President: An-Yeu (Andy) Wu
- President - Elect: Yoshifumi Nishio
- Past President: Myung Hoon Sunwoo
- Vice President - Financial Activities: Jinwook Burm
- Vice President - Conferences: Kea-Tiong (Samuel) Tang
- Vice President - Publications: Gabriele Manganaro
- Vice President - Regional Activities and Membership: Yongfu Li
- Vice President - Technical Activities: Hanho Lee
- Vice President - Education and Communications: Fakhrul Zaman Rokhani
- Vice President - Industry: Rajiv Joshi

Board of Governors (BoG)

2024-2026 Member at Large	2025-2027 Member at Large	2026-2028 Member at Large
• Pamela Abshire	• Chia-Wen Lin	• Jose M. de la Rosa
• Kyung Ki Kim	• Erika Covi	• Alex James
• Yoko Uwate	• Victor Grimblatt	• Francois Rivet
	• Yajun Ha	• Sorin Cotofana
	• Keshab K.Parhi	• Xinmiao Zhang

Regional Member at Large

- R1-7 Regional Member at Large (2024 - 2026): Jennifer Blain
- R9 Regional Member at Large (2024 - 2026): Carlos Silva-Cardenas
- R8 Regional Member at Large (2026 - 2028): Maurizio Valle
- R10 Regional Member at Large (2026 - 2028): Ittetsu Taniguchi

Appointed Members & Representatives

- Appointed Young Professionals Member (2025 - 2026): Bokyung Kim
- Appointed Women in Engineering Member (2026 - 2026): Hai (Helen) Li
- SSCS Representative to CASS (2026 - Present): Amara Amara

Circuits and Systems Society Editors

IEEE Transactions on Circuits and Systems I: Regular Papers

- **Editor-in-Chief: Jose M. de la Rosa**
- **Associate Editor-in-Chief: Xinmiao Zhang**

IEEE Transactions on Circuits and Systems II: Express Briefs

- **Editor-in-Chief: Edoardo Bonizzoni**
- **Associate Editor-in-Chief: Antonio Liscidini**

IEEE Transactions on Circuits and Systems for Video Technology

- **Editor-in-Chief: Shan Liu**
- **Deputy Editor-in-Chief: Stefano Berretti**

IEEE Transactions on Biomedical Circuits and Systems

- **Editor-in-Chief: Pedram Mohseni**
- **Associate Editor-in-Chief: Arindam Basu**

IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)

- **Editor-in-Chief: Chi-Tsun (Ben) Cheng**
- **Associate Editor-in-Chief: Erivelton Nepomuceno**

IEEE Transactions on Very Large Scale Integration (VLSI) Systems

- **Editor-in-Chief: Victor Grimblatt**

IEEE Transactions on Artificial Intelligence

- **Editor-in-Chief: Yiran Chen**

IEEE Open Journal of Circuits and Systems

- **Editor-in-Chief: Nicole McFarlane**
- **Associate Editor-in-Chief: Alex James**

IEEE Circuits and Systems Magazine

- **Editor-in-Chief: Keshab Parhi**
- **Associate Editor-in-Chief: Andreas Demosthenous**

IEEE Gustav Robert Kirchhoff Award

- **2026 IEEE Gustav Robert Kirchhoff Award *Sponsored by the IEEE Circuits and Systems Society***
- **Behzad Razavi For fundamental contributions to the analysis and design of high-speed analog and radio-frequency integrated circuits.**

Conference Sponsors & Exhibitors

Platinum Elite Sponsors

Gold Premium Sponsors

Basic Professional Sponsors

Social Events Guide

Welcome Reception

Date & Time:

Sunday, May 24, 18:00 - 21:00

Location:

Pearl Hall & Foyer, Shanghai Min, SHICC, Level 7

WiCAS-YPCAS Event

Date & Time:

Monday, May 25, 18:00-21:30

Location:

Europe Hall, SHICC, Level 5

Gala Banquet

Date & Time:

Tuesday, May 26, 19:00 - 21:00

Location:

Grand Ballroom 1, SHICC, Level 7

Dress Code:

Smart Casual or Business Attire

Highlights:

The evening will feature the Awards Ceremony alongside a showcase of traditional Chinese cultural performances.

- **Face Changing (Bian Lian):** A breathtaking masterpiece of Sichuan Opera.
- **Chinese Acrobatics:** A stunning display of balance, flexibility, and strength.
- **Martial Arts (Wushu):** A powerful demonstration of traditional Chinese Kung Fu.

Farewell Reception: Huangpu River Cruise

Date & Time: Wednesday, May 27, 18:00 - 20:30

17:40 Group Departure from Venue (10-min walk)

18:00 Cruise Departure

Location: Oriental Pearl Tower Wharf

Keynote Speakers

Keynote Speaker 1

Monday, May 25, 2026 | 09:00-10:00 | Morning Session

Tingbo He

President of HUAWEI Semiconductor, Director of HUAWEI Scientist Committee, China

Topic: New Semiconductor Path in Practice

Abstract： As semiconductor scaling-down approaches the lithographic and fundamental atomic limits, the Moore's Law and Dennard's Law, once have governed the evolution of the semiconductor industry for decades, are becoming much less effective. Without device shrinking as the main lever, how can capability and performance continue to scale? The question stays open. Some face this challenge today; the rest of the industry will face the same challenge five to ten years down the road-which makes finding an answer all the more important. How can we provide a new sustainable scaling path? How can the theoretical approach be applied in practice? Through the past five-year's exploration involving the rigorous design and delivery of successful commercialization of more than 150 advanced chips, Huawei Semiconductor has thoroughly investigated the future-oriented design methodologies for electronic systems and discovered the rules that drive the system evolution for semiconductor devices. These rules not only provide theoretical bases on the technology evolution in the post-Moore era, but also can be used as new references for SoC design, manufacturing process, and the evolution path of the semiconductor industry over the next decade.

Biography： He Tingbo is an electrical engineer by training and a chip designer by practice. Over the last 22 years, she has led Huawei Semiconductor's growth from a small in-house chip design department into one of the world's largest semiconductor workforce-by technology diversity and depth, and by far the widest portfolio of chip products globally.

Her career can be seen in two stages.In the first stage, she built both the full capabilities and the full product portfolio-and the two supported each other. She saw clearly that to build a world-class workforce, you need a full set of technologies in your toolbox. Under her leadership, Huawei Semiconductor developed large-scale SoC capability, high-speed analog and mixed-signal I/O, radio frequency circuits, electron-optical capabilities, advanced packaging, power and sensor capabilities, supply chain management, the ability to work with leading logic foundries and advanced memory technologies, 3D IC, and the full range of processor technologies-CPU, GPU, NPU, network processors, DSP, and domain-specific architectures. In parallel, she built the widest product portfolio in the industry: mobile phones, AI, general-purpose and AI processors, telecommunications and networking, and consumer electronics. Capabilities enabled the portfolio; the portfolio drove demand and learning that strengthened the capabilities. By leading an organization that competes relentlessly with industry leaders in every one of these sectors, she built products that rival the combined portfolio of the chip giants of Silicon Valley. That rich portfolio has enabled Huawei to provide broad and valuable services and products to its customer base and fueled a positive cycle-reinvesting in R&D and next-generation products, which in turn drive further growth.

In the second stage, her company was the first to face the difficulty in device shrinking-something that others may encounter only in five to ten years down the road. He Ting Bo reinvigorated her team to find a new path and recover from that dire situation. In the last six years they have recreated over 150 designs using a new approach. This has enabled Huawei to come back on stage with world-class products and services. Her unique experience offers useful lessons for others to examine and study-and she will share more, in her talk today.

Keynote Speaker 2

Monday, May 25, 2026 | 13:30-14:30 | Afternoon Session

M. Jamal Deen

Distinguished University Professor, Dr. Haykin Distinguished Engineering Professor
Director of the Micro- and Nano-Systems Laboratory (MNSL)
McMaster University, Canada

Topic: Unprecedented Vision-From Single-photon Detectors and Pixels to Engineering and Health Systems

Abstract：Unprecedented vision systems capable of sensing, timing, and interpreting individual photons are rapidly reshaping applications that span engineering, autonomy, and healthcare. At the core of this transformation are single-photon avalanche diodes (SPADs) and their tight integration with advanced silicon circuits, modeling frameworks, and system architectures. This presentation will trace a trajectory from device-level physics and pixel engineering to large-scale sensing and health systems enabled by single-photon technologies. We first highlight recent advances in physics-based SPAD modeling, including compact Verilog-A descriptions of noise and calibrated photon detection probability models that accurately capture process, optical stack, and variability effects. These models provide predictive, simulator-compatible tools essential for noise-aware co-design of SPADs and readout circuits. We then examine circuit and pixel innovations, such as high-speed quench and reset schemes, time-gated and clock-driven operation, and integrated time-to-digital converters that push timing resolution into the picosecond regime while mitigating dead time, afterpulsing, and intersymbol interference. Building on these foundations, we discuss system-level realizations, including SPAD-based optical wireless communication receivers, automotive LiDAR sensors, and time-resolved biomedical imagers, where single-photon sensitivity translates directly into extended range, improved robustness, and enhanced diagnostic capability. By unifying device physics, compact modeling, circuit architectures, and application-driven system design, this work illustrates how single-photon detectors are evolving from isolated pixels into enabling platforms for next-generation engineering and health systems, offering unprecedented vision across scales, ranging from individual photons to complex real-world environments.

Biography：Dr. M. Jamal Deen is a Distinguished University Professor, Dr. Haykin Distinguished Engineering Professor and Director of the Micro- and Nano-Systems Laboratory (MNSL), McMaster University. As an educator, he won the SM Sze Education Award from IEEE Electron Devices Society (inaugural winner), the Ham Education Medal from IEEE Canada, the McMaster University President's Award for Excellence in Graduate Supervision, and MSU Macademics' Lifetime Achievement Award for his exceptional dedication to teaching and significant contribution to student life, the community at large, and academia.Dr. Deen served as the elected President of the Academy of Science, The Royal Society of Canada in 2015-2017. Currently, he is serving as the inaugural elected Vice President (North) of The World Academy of Sciences, representing the developed countries. His current research interests are nanoelectronics, optoelectronics, nanotechnology, data analytics and their emerging applications to health and environmental sciences. Dr. Deen's research record includes more than 930 peer-reviewed articles (about 20% are invited), two textbooks on "Silicon Photonics- Fundamentals and Devices" and "Fiber Optic Communications: Fundamentals and Applications", 13 awarded patents of which 7 are/were extensively used in industry, and twenty-seven best paper/poster/presentation awards.

As an undergraduate student at the University of Guyana, Dr. Deen was the top ranked mathematics and physics student and the second ranked student at the university, winning the Irving Adler prize and the Chancellor's gold medal, respectively. As a graduate student, he was a Fulbright-Laspau Scholar and an American Vacuum Society Scholar. He is a Distinguished Lecturer of the IEEE Electron Device Society for more than two decades now. His awards and honors include the Callinan Award as well as the Electronics and Photonics Award from the Electrochemical Society; a Humboldt Research Award from the Alexander von Humboldt Foundation; the Eadie Medal from the Royal Society of Canada; McNaughton Gold Medal, the Fessenden Medal and the Gotlieb Computer Medal, all from IEEE Canada. In addition, he was awarded the five honorary doctorate degrees in recognition of his exceptional research, scholarly and educational accomplishments, exemplary professionalism and valued services.Dr. Deen has been elected by his peers as Fellow/Academician of fourteen national academies and professional societies including The Royal Society of Canada; Academician (Foreign Member) of The Chinese Academy of Sciences; The World Academy of Sciences, National Academy of Sciences India; The African Academy of Sciences; The American Physical Society; and The Electrochemical Society (FECS). He was also elected to the Order of Canada, the highest civilian honor awarded by the Government of Canada.

Keynote Speaker 3

Tuesday, May 26, 2026 | 09:00-10:00 | Morning Session

Jian-Wei Pan

Vice President, University of Science and Technology of China (USTC), China

Topic:Quantum Network: Quantum Communication, Computation, and Metrology

Abstract：With the continued development of quantum information science, it is anticipated that large-scale quantum networks will be established. Such networks are expected to enable ultra-precise information sensing through quantum metrology, secure and efficient information exchange via quantum key distribution (QKD) and quantum teleportation, and rapid information processing through quantum computing. However, turning quantum networks from theoretical concepts into practical reality still faces numerous technical challenges. Achieving secure long-distance quantum communication requires addressing security issues under realistic conditions and overcoming the inherent loss in optical fibers, while building quantum computers demands solving the challenge of scalable and precise manipulation of qubits.

In this talk, I review our two-decade efforts toward quantum networks, including: developing decoy-state QKD and measurement-device-independent (MDI) QKD to close device imperfections loopholes; progressing quantum repeaters and satellites to extend communication range; using photon coherent manipulation techniques developed from quantum communication to demonstrate quantum computational advantage; employing ultracold atoms in optical lattices for quantum simulations of complex systems, advancing near-term quantum computing applications; surpassing the surface code quantum error correction threshold; and developing high-precision optical lattice clocks using ultracold atom technology. Future prospects include building a global quantum communication network using efficient constellations and geostationary orbit (GEO) satellites. This will also support advanced quantum metrology, potentially redefining the SI second. In quantum computation, our five-year plan targets practical quantum simulators to study high-temperature superconductivity, quantum Hall effect, etc. Over the next 10–15 years, scaling to millions of qubits with quantum error correction may lay the foundation for universal quantum computers.

Biography：Prof. Jian-Wei Pan, born in Mar, 1970, is a full professor of physics at the University of Science and Technology of China. He obtained his Ph.D. degree in 1999 from the University of Vienna. In 2011, he was elected as the academician of Chinese Academy of Sciences. He is also a foreign member of the Austrian Academy of Sciences, the Royal Society (London), and a TWAS Fellow.

Prof. Jian-Wei Pan's research fields focus on quantum foundations, quantum optics and quantum information. As one of pioneers in experimental quantum information science, he has accomplished a series of profound achievements including: constructing the first integrated space-ground quantum communication network by combining the Micius quantum satellite with optical fiber backbones; demonstrating quantum computational advantage; realizing quantum simulations of multiple complex systems using ultracold atoms; and surpassing the surface code quantum error correction threshold. He has authored more than 460 peer-reviewed publications including 3 in Rev. Mod. Phys. and 41 in Nature/Science, with more than 98,000 citations. He has received numerous honors, including the Fresnel Prize of the European Physical Society, the Qiu Shi Outstanding Scientist Award, the International Quantum Award from the International Conference for Quantum Communication, Measurement and Computing (QCMC), the Ho Leung Ho Lee Prize for Scientific and Technological Achievement, the First Class Prize of the State Natural Science Award, the Future Science Prize in Physical Sciences, the R. W. Wood Prize from the OSA, the Micius Quantum Prize, and the Zeiss Research Award, the Tengchong Science Award, the UNESCO Mendeleev International Prize in the Basic Sciences, among others.

Keynote Speaker 4

Tuesday, May 26, 2026 | 13:30-14:30 | Afternoon Session

Giovanni De Micheli

Scientific Director, EcoCloud Center

EPFL Lausanne, Switzerland

Topic: Taming the Dragon: Circuits and Systems for Energy-Efficient and Secure Computation

Abstract：The unprecedented increase in computation requirements by AI/ML applications, and its cost in term of electrical energy and heat disposal, create a formidable challenge in view of the non-negotiable protection of our planet. At the same time, the data deluge and the proliferation of smart software systems in everyday and everyone's life pose another challenge in view of the required protection of our privacy. The design of new computation and communication systems has to address these needs by leveraging devices, circuits and architectures within a comprehensive vision to fulfill the growth a sustainable planet and a respectful society.

Biography：Giovanni De Micheli is a research scientist in electronics and computer science. He is credited for the invention of the Network on Chip design automation paradigm and for the creation of algorithms and design tools for Electronic Design Automation (EDA). Prof. De Micheli is the Scientific Director of the EcoCloud center at EPFL Lausanne, Switzerland. Previously, he was Professor of Electrical Engineering at Stanford University, Director of the EPFL LSI Laboratory, Director of EPFL Electrical Engineering Institute at EPFL and leader of the Swiss Federal Nano-Tera.ch program. He is a Fellow of ACM, AAAS and IEEE, a member of the Academia Europaea, of the Swiss Academy of Engineering Sciences (SATW) and International Honorary member of the American Academy of Arts and Sciences. He is the recipient of the 2025 IEEE Gustav Kirchhoff Award, the 2022 ESDA-IEEE/CEDA Phil Kaufman Award, and several other awards.

Keynote Speaker 5

Wednesday, May 27, 2026 | 09:00-10:00 | Morning Session

Howard C. Yang

Chairman & CEO, Montage Technology, China

Topic: From Memory-Constrained to Memory-Optimized: How Engram Conditional Memory + MRDIMM/CXL Reshapes Sparse AI Architectures

Abstract： At the dawn of 2026, DeepSeek-AI published the engram module which marks the birth of the memory-dominant large language models. Traditional Transformers with attention and MoE lack efficient native knowledge lookup, forcing repeated expensive recomputation of static patterns (common phrases, entities, local dependencies) and wasting depth and cycles. Engram introduces conditional memory as a new sparsity axis: modernized N-gram embeddings enable O(1) deterministic lookups, offloading static knowledge to scalable parameterized tables (100B+ parameters). The Transformer backbone focuses solely on dynamic global reasoning and long-range dependencies. Its infrastructure-aware design achieves near-zero-overhead DRAM prefetching follows a U-shaped scaling law, and delivers outsized gains: Engram-27B outperforms MoE baselines at matched FLOPs with power-law "infinite memory" scaling.

This exposes AI's next bottleneck: memory access patterns, tail latency, and organization -- no longer peak FLOPS. MRDIMM delivers a bandwidth uplift and lower latency for Engram's random, high-concurrency accesses, enabling robust O(1) lookups in demanding inference scenarios. CXL provides disaggregated, pooled, coherent memory pools across nodes, allowing massive Engram tables to reside in shared memory -- eliminating replication, bypassing HBM limits, and (with compression) doubling effective capacity at lower TCO. Together, Engram + MRDIMM + CXL forge a genuinely memory-first sparse AI paradigm: computation specializes in deep reasoning, while memory specializes in high-speed storage and retrieval of knowledge -- finally circumventing the GPU memory wall and unlocking the next phase of efficient, scalable intelligence.

Biography： Dr. Howard C. Yang co-founded Montage Technology in 2004 and has served as its Chairman and CEO since its inception. From 1990 to 1994, Dr. Yang was engaged in integrated circuit (IC) R&D and design at National Semiconductor Corp. and other Silicon Valley companies. In 1994, he returned to China and established the country's first IC design center employing modern design methodologies. In 1997, he co-founded Newave Semiconductor Corp., China's first venture capital-backed IC design company, which later merged with a major U.S. semiconductor firm in 2001 -- a transaction ranked among China's top ten mergers of the year. Dr. Yang is an IEEE Life Fellow and has received several distinguished awards, including the IEEE CAS Industrial Pioneer Award, the JEDEC Distinguished Executive Leadership Award, and the Magnolia Gold Award from the Shanghai Municipal Government. He holds M.S. and Ph.D. degrees in Electrical and Computer Engineering from Oregon State University and was inducted into its Engineering Hall of Fame in 2024.

Tutorial

Overview

May 24th, Morning (08:30 A.M. ~ 12:00 A.M.)		
T1	From Circuits to Startups: Translating Innovation into Impact (Entrepreneurship Tutorial)	5B+5C
T2	AI-Enhanced Implementation of High-Efficiency Delta-Sigma ADCs	5H
T5	CoDeCAS: Co-designing Devices, Circuits, Systems and Algorithms for Uncertainty aware Multimodal Artificial Intelligence at the Edge	Yangtze Hall
T6	Power electronic circuits-based safety enhancement techniques for lithium-ion batteries	5F
T7	High-Throughput Neural Signal Acquisition: Hardware Implementation and Bio-Inspired Approaches	5A
T8	Advancing Spatial Intelligence - Geometric Modeling, Representation Learning, and 3D Compression	5I
T9	From SNNs to Silicon: Automated hardware deployment of spiking neural networks	5D+5E
T16	Mm-Wave to THz Signal Generation in CMOS: An Injection Locking Approach	5J
May 24th, Afternoon (13:30 P.M. ~ 17:00 P.M.)		
T4	Towards 6G UWB Signal Processing Chain Design	5F
T10	Low-voltage frequency generation, modulation, and demodulation circuits for mobile IoT	5D+5E
T11	Visual Signal Processing from Human to Embodied Intelligence	Yangtze Hall
T12	Intelligent Design of Wireless Power Transfer: From Fundamentals to AI-Driven Frameworks	5I
T13	Optical Biotelemetry Systems: Basics and Advances for Wireless Data and Power Transmission in Biomedical Implants	5H
T14	Leveraging IEEE DataPort and IEEE Data Descriptions for Enhanced Research Impact and Student Engagement	5J
T15	Modern Power Amplifier Design: From Classical Principles to AI-Assisted Optimization	5A
T17	Efficient Learning-based Models for Multimodal Data Compression	5B+5C

Morning Session (8:30 A.M. ~ 12:00 A.M.)

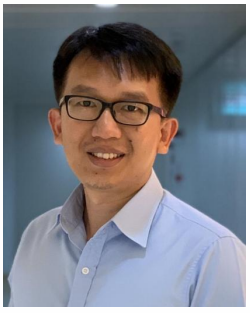
Tutorial 1

From Circuits to Startups: Translating Innovation into Impact

Sunday, May 24, 2026 | 08:30 – 12:00 (Morning) | Location: 5B+5C

Jie Chen
(***Fudan University, China***)

Michael Friebe
(***AGH University of Krakow, Poland***)



Fakhrul Zaman Rokhani
(***University of Minnesota, USA***)

Abstract: This tutorial aims to equip researchers, engineers, and students in the circuits and systems (CAS) community with practical entrepreneurial skills to identify, validate, and subsequently translate technical innovation into real-world impact. While ISCAS provides a premier platform for advancing scientific and engineering knowledge, there is a growing need for guidance on identifying commercialization opportunities, developing sustainable business models, and navigating funding and startup ecosystems. The session will cover key aspects of technology entrepreneurship - including opportunity recognition, intellectual property strategy, market validation, and venture creation - illustrated through case studies relevant to circuits and systems innovations. Participants will gain not only foundational frameworks but also actionable insights to bridge the gap between research excellence and entrepreneurial success. The participants will also receive a checklist and relevant large language model (LLM) prompts.

Schedule

Time	Content
08:30 - 09:20	Opportunity recognition introduction
09:20 - 10:10	Intellectual property strategy introduction
10:10 - 10:30	Coffee break
10:30 - 11:20	Market validation introduction
11:20 - 12:00	Venture creation

Tutorial 2

AI-Enhanced Implementation of High-Efficiency Delta-Sigma ADCs

Sunday, May 24, 2026 | 08:30 – 12:00 (Morning) | Location: 5H

Liang Qi
(Shanghai Jiao Tong University, China)

José M. de la Rosa
(University of Seville, Spain)

Abstract: High-efficiency oversampling analog-digital converters (ADCs) are still at the forefront of integrated circuits and very popular when it comes to research and development, both in industry and academia. While their implementation as noise-shaping SAR ADCs comes with the drawback of driving a large sampling capacitor merged with the capacitive DAC, the delta sigma modulator (DSM) based converter omits this. Their application range is huge, from wideband wireless communications to the data acquisition in IoT sensor nodes that demands an ultra-high resolution with very low power consumption. Due to the available high integrator gain within the signal bandwidth and the feedback established by the oversampling converters, they can achieve a relatively high signal-to-noise-and-distortion ratio (SNDR) and spurious-free-dynamic-range (SFDR), within the signal band of interest. The ability to shape the unwanted noise and errors to the out-of-the-band gains a substantial design degree of freedom to the oversampling converters compared to their Nyquist counterparts. DSM is found in two basic categories: Discrete-Time (DT) DSM with excellent accuracy and also excellent power efficiency in recent dynamic implementations. Continuous-Time (CT) DSM comes with important benefits of inherent anti-aliasing filtering, easier drivability, and power-efficient implementation due to the continuous-time signal processing. Moreover, the architectural diversity of DSM has steadily increased over the last decades, beyond others employing various kinds of multi-stage designs, and incremental DSM have recently again gained an increasing attention. Circuit designers should understand the underlying trade-offs in detail before they can make the correct design decisions.

This tutorial will provide a detailed review of the fundamentals, important decision-making factors, recent trends and advanced design techniques, and future perspectives on the state-of-the-art oversampling delta-sigma converters, spanning a range from DT to CT, free-running and incremental one. Moreover, regarding the practical implementation, we will go through the classical methods, covering the optimization-based loop-filter design, and then guide the audience through the most recent advances of AI-based synthesis and implementation of DSMs, both on systems and circuitry levels.

Schedule

Time	Content
08:30 - 10:10	1) The principle of delta-sigma ADC; 2) The implementation methodology: DT vs. CT; 3) Architectural choices; 4) Incremental operation
10:10 - 10:30	Coffee break
10:30 - 12:30	1) An overview of classical loop-filter scaling method and automated design/optimization of DSMs; 2) Main practical aspects, pros and cons, of AI-assisted design; 3) Introduction to an AI-assisted DSM synthesis toolbox; 4) A comparison to other optimization methods

Tutorial 5

CoDeCAS: Co-designing Devices, Circuits, Systems and Algorithms for Uncertainty aware Multimodal Artificial Intelligence at the Edge

Sunday, May 24, 2026 | 08:30 – 12:00 (Morning) | Location: Yangtze Hall

Amit Ranjan Trivedi
(***University of Illinois at Chicago, USA***)

Priyesh Shukla
(***International Institute of Information Technology, India***)

Abstract: Uncertainty awareness in language and vision AI models are essential for robust decision making in critical real-time tasks at the Edge such as autonomous drone surveillance, and AR/VR-assisted healthcare. Model predictions often suffer from data, sensor and environmental imperfections leading to inaccurate decision making that is unacceptable in safety critical tasks. Various probabilistic AI techniques such as Monte-Carlo Dropout, Variational inference, Deep ensembles and Conformal predictions enable uncertainty awareness in the AI model predictions. However, challenges to deep learning inference at the Edge further aggravates with incorporation of prediction uncertainties due to multifold increase in compute and power requirements. We uniquely address these challenges all the way from novel device technology to circuits, architectures and co-designed algorithms, thus navigating the audience to the full stack research techniques and hardware/software co-design frameworks towards building sustainable as well as robust circuits and systems for modern AI processing.

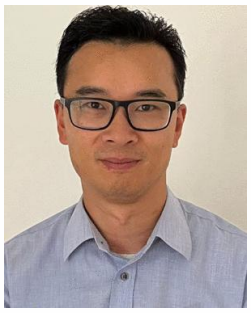
Schedule

Time	Content
08:30 - 09:00	Motivation of uncertainty-awareness in LLMs, SLMs, VLMs, CNNs from application case studies
09:00 - 09:30	Basics of uncertainty-aware (probabilistic) methods
09:30 - 10:10	Devices - Gaussian transistors and memtransistors for probabilistic ML
10:10 - 10:30	Coffee break
10:30 - 11:00	Circuits and architectures - Compute-in-Memory acceleration for probabilistic ML
11:00 - 11:30	Co-design with device/hardware characteristics and constraints
11:30 - 12:00	Impact on sustainable and robust edge systems, plus Q&A

Tutorial 6

Power electronic circuits-based safety enhancement techniques for lithium-ion batteries

Sunday, May 24, 2026 | 08:30 – 12:00 (Morning) | Location: 5F



Zhaoyang Zhao
(***Southwest Jiaotong University, Chengdu, China***)

Herbert Ho-Ching Iu
(***University of Western Australia, Australia***)

Lizhou Liu
(***Sichuan University, China***)

Abstract: Safety enhancement for lithium-ion batteries (LIBs) has received a lot of attention from academic and industrial fields. However, there is a lack of attention from the perspective of the application power electronics (PEs) in the systems. This tutorial gives a presentation about PE-based safety enhancement technologies for LIBs, mainly focusing on battery management. It introduces the latest advances in battery protection, balancing, monitoring, and lifetime improvement, all based on PE technologies. Detailed discussion and future research opportunities are given. This tutorial aims to provide a reference for PE researchers who want to make some efforts in LIB safety.

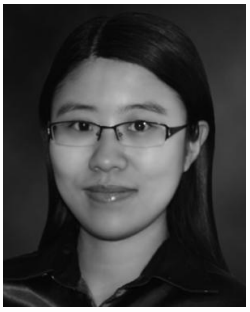
Schedule

Time	Content
08:30 - 09:00	Introduction and overview
09:00 - 09:30	PE-based battery protection techniques
09:30 - 10:10	PE-based online monitoring techniques
10:10 - 10:30	Coffee break
10:30 - 11:00	PE-based lifetime improvement techniques
11:00 - 12:00	PE-based battery balancing techniques

Tutorial 7

High-Throughput Neural Signal Acquisition: Hardware Implementation and Bio-Inspired Approaches

Sunday, May 24, 2026 | 08:30 – 12:00 (Morning) | Location: 5A



Milin Zhang
(***Tsinghua University, China***)

Donhee Ham
(***Harvard University, USA***)

Abstract: This tutorial session explores cutting-edge advancements in neural signal sensing and neuromorphic engineering, with a focus on hardware implementation and bio-inspired design principles. The session will discuss the challenges and solutions for high-throughput neural signal wireless sensing, emphasizing circuit design methodologies and ultra-low-power implementations, as well as the evolution of neuromorphic engineering from strict brain mimicry to bio-inspired designs, with a vision for copy-and-paste approaches that map functional synaptic connectivity onto silicon circuits. This session will provide attendees with a comprehensive understanding of how hardware innovations are driving advancements in neural signal processing and neuromorphic systems, enabling applications in low-power computing, adaptive learning, and cognitive systems.

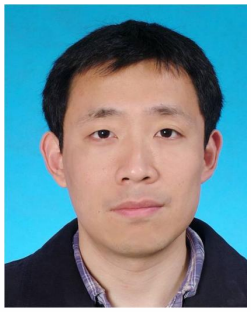
Schedule

Time	Content
08:30 - 10:10	Introduction to High-Throughput Wireless Neural Signal Sensing
10:10 - 10:30	Coffee break
10:30 - 12:00	Population-Scale Intracellular Recording and Biologically Grounded Neuromorphic Systems

Tutorial 8

Advancing Spatial Intelligence —— Geometric Modeling, Representation Learning, and 3D Compression

Sunday, May 24, 2026 | 08:30 – 12:00 (Morning) | Location: 5I



Junhui Hou
(*City University of Hong Kong, China*)

Weiyao Lin
(Shanghai Jiao Tong University, China)

Abstract: 3D spatial intelligence - the capacity to perceive, reason about, and manipulate geometric data - is increasingly vital for advancing artificial intelligence applications across various domains, including robotics, metaverse, immersive telepresence, and autonomous systems. This tutorial aims to provide a comprehensive overview of recent advancements in the field, covering critical aspects from geometric modeling to 3D representation learning and 3D compression (especially 3D Gaussian compression) techniques.

Schedule

Time	Content
08:30 - 09:30	3D Geometric Modeling and Representation
09:30 - 10:10	Augmented 3D Representation Learning with 2D Modalities/Structures
10:10 - 10:30	Coffee break
10:30 - 12:00	Compression of 3D Gaussian Representation

Tutorial 9

From SNNs to Silicon: Automated hardware deployment of spiking neural networks

Sunday, May 24, 2026 | 08:30 – 12:00 (Morning) | Location: 5D+5E

Michail Rontionov
(***University of Southampton, UK***)

Dr. Jens Egholm Pedersen
(***Technical University of Denmark, DK***)

Abstract: Brain-inspired spiking neural networks promise 3–4 orders of magnitude energy savings compared to conventional neural network implementations. SNNs combine continuous neuron dynamics with discrete spike communication, enabling rich temporal computation with efficient, event-driven information transfer—these are among the key ingredients allowing the human brain to operate on approximately 20 watts.

This tutorial provides an overview of unrolling SNNs defined in a collection of simulators into FPGA bitstreams via a customisable, open-source toolchain. We introduce a direct compilation framework that translates SNN models into FPGA bitstreams: participants will convert an existing spiking convolutional network to hardware, then train and optimise their own architecture. Participants will learn to program FPGA accelerators for SNNs and gain practical skills in mapping conventional network architectures into the spiking domain. This toolchain also serves as a stepping stone toward open-source neuromorphic ASIC development.

Schedule

Time	Content
08:30 - 09:20	Introduction to neuromorphic accelerators
09:20 - 10:10	Building and training quantized SNNs in JAX
10:10 - 10:30	Coffee break
10:30 - 11:00	Mapping NIR to FPGA with SpinalHDL
11:00 - 12:00	Hands-on running NIR networks on FPGA

Tutorial 16

Mm-Wave to THz Signal Generation in CMOS: An Injection Locking Approach

Sunday, May 24, 2026 | 08:30 - 12:00 (Morning) | Location: 5J

Jingzhi Zhang
(***University of Electronic Science and Technology of China, China***)

Xiaolong Liu
(***Southern University of Science and Technology, China***)

Abstract: Moving to higher frequencies become a consensus in communication and radar society for wider bandwidth and smaller form factor, thereby gestating new applications spread from mm-wave to THz frequency bands, including 5G new radio (NR), 6G communication, automotive radar, and THz sensing. Unlike the traditional high-frequency signal generation in vacuum tube, which inherently has high power and low phase noise, new demands on power, size, and cost force the signal generation to be fully integrated on a silicon chip, but with sacrificed performances.

In this tutorial, we focus on the fundamental limitations of signal generation in CMOS from mm-wave to THz frequencies, and the design trade-offs among operating frequencies, bandwidth, phase noise, and power consumption. We will introduce new signal generation topologies based on an injection-locking technique and discuss the design methodology of high-frequency signal generators. This tutorial includes discussion of fundamental problems on silicon-based high-frequency signal generation, design of silicon-based oscillators and phase-locked loops (PLL), introduction of the injection-locking technique and how does it benefit for high-frequency signal generations, design examples of mm-wave and THz injection-locked signal sources, and their applications in communication and radar systems.

Schedule

Time	Content
08:30 - 09:10	Background, review of mm-wave/THz signal generation, injection-locking technique, and mm-wave implementations
09:10 - 09:30	Coffee break
09:30 - 10:30	THz injection-locked oscillators, oscillators/PLLs, conclusion and discussion
10:30 - 11:00	Questions and discussions

Afternoon Session (13:30 P.M. ~ 17:00 P.M.)

Tutorial 4

Towards 6G UWB Signal Processing Chain Design

Sunday, May 24, 2026 | 13:30 – 17:00 (Afternoon) | Location: 5F

Abdel Martinez Alonso
(***Tech Idea , Japan***)

Francois Rivet
(***University of Bordeaux , France***)

Rodney Martinez Alonso
(***KU Leuven , Belgium***)

Abstract: The evolution toward 6G networks is driven by the demand for extreme bandwidth to support machine-type communications, holographic experiences, and immersive reality. Achieving this requires energy-efficient transceiver architectures capable of handling ultra-wideband signals well beyond the limits of 5G. A central challenge lies in data converters, where higher sampling rates lead to an increase in both noise and power consumption.

This half-day tutorial, “Towards 6G UWB Signal Processing Chain Design,” presents advances in interleaved architectures and frequency-domain approaches based on Walsh transformations. It covers the design of interleaved data converters, Walsh-based transceivers, and AI-driven applications, including spectrum sensing and interference mitigation. Participants will gain a comprehensive understanding of the signal processing chain from core principles to advanced circuit-level solutions, focusing on energy efficiency, parallelization, and system-level performance.

Schedule

Time	Content
13:30 -14:20	Introduction to Efficient Data Converters Design
14:20 - 15:10	Life beyond OFDM: Walsh domain encoding
15:10 - 15:30	Coffee break
15:30 - 17:00	From Theory to Impact: AI-Driven Applications of Walsh-Based Transceivers

Tutorial 10

Low-voltage frequency generation, modulation, and demodulation circuits for mobile IoT

Sunday, May 24, 2026 | 13:30 – 17:00 (Afternoon) | Location: 5D+5E

Woogeun Rhee

(***Sungkyunkwan University, Korea***)

Abstract: As future wireless systems leveraging advanced CMOS technologies demand not only low-power but also low-voltage design, robust frequency generation, modulation and demodulation have become more critical than ever. In particular, sub-0.5V frequency synthesis and modulation are essential to enable battery-free operation in mobile IoT devices, as they can be directly powered by energy harvesters without requiring additional DC-DC converters. However, designing a low-voltage fractional-N PLL is highly challenging, since both matching and linearity degrade significantly as the supply voltage is scaled down.

This half-day tutorial reviews the state-of-the-art PLL architectures and presents fully voltage-mode PLL and transceiver architectures that operate under a 0.5V supply voltage. In addition, the extensive use of single-bit modulation and demodulation techniques for the robust design of ultra-low-voltage transmitters and receivers will be discussed.

Schedule

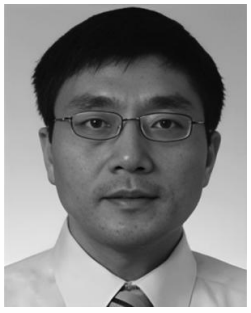
Time	Content
13:30 - 14:00	Introduction
14:00 - 14:30	Single-bit delta-sigma modulation for frequency generation and modulation
14:30 - 15:10	Voltage-mode hybrid fractional-N PLLs and transmitters
15:10 - 15:30	Coffee break
15:30 - 16:20	Low-voltage receivers
16:20 - 17:00	Design challenges and future considerations

Tutorial 11

Visual Signal Processing from Human to Embodied Intelligence

Sunday, May 24, 2026 | 13:30 – 17:00 (Afternoon) | Location: Yangtze Hall

Chunyi Li
(***Center of AI Evaluation,China***)



Weisi Lin
(***Nanyang Technological University, Singapore***)

Zicheng Zhang
(***Shanghai AI Lab, China***)

Huiyu Duan
(***Shanghai Jiao Tong University, China***)

Jianbo Zhang
(***Xinjiang University, China***)

Guangtao Zhai
(***Shanghai Jiao Tong University, China***)

Abstract: This tutorial explores the cutting-edge intersection of human visual perception and embodied intelligence, bridging the gap between biological Human Visual System (HVS) and Robotic Visual System (RVS). We will examine how visual signal processing principles derived from human can be adapted and enhanced for embodied intelligence, such as image compression, restoration, and quality assessment, enabling more efficient embodied task execution. The tutorial covers fundamental concepts in visual perception, advanced signal processing techniques, and practical applications in embodied intelligence, with particular focus on how large language models can be integrated with visual processing for enhanced embodied capabilities.

Schedule

Time	Content
13:30 - 14:20	Intelligence Visual Perception Loop
14:20 - 15:10	Traditional Visual Signal Processing for Human
15:10 - 15:30	Coffee break
15:30 - 17:00	Visual Signal Processing for Embodied Intelligence

Tutorial 12

Intelligent Design of Wireless Power Transfer: From Fundamentals to AI-Driven Frameworks

Sunday, May 24, 2026 | 13:30 – 17:00 (Afternoon) | Location: 5I

Hiroo Sekiya
(***Chiba University, Japan***)

Xiuqin Wei
(***Chiba Institute of Technology, Japan***)

Abstract: Wireless Power Transfer (WPT) has attracted significant attention as an innovative technology enabling a wide range of applications, from consumer electronics and electric vehicles to industrial robotics. The development of efficient and reliable WPT systems, particularly in the MHz frequency range, requires the integrated consideration of circuits, magnetic coupling, electric-field coupling, and control. Conventional design approaches, largely dependent on expert knowledge and trial-and-error prototyping, face inherent limitations: they struggle to address fundamental challenges such as output fluctuation and efficiency degradation caused by load variation and coil misalignment, thereby restricting scalability and innovation.

This tutorial will provide both the fundamentals and the latest advancements in WPT, with a special focus on methods that fundamentally overcome these challenges. Beginning with the principles of inductive and electric-field (capacitive) coupling, the tutorial will cover advanced load-independent topologies and our uniquely developed AI-driven design methodologies, characterized by fully numerical optimization, high-accuracy modeling, and the integrated design of physical coil models with circuit component values. Beyond serving as a powerful design tool, these approaches represent a novel framework for principle-driven analysis and knowledge discovery in WPT system design. Practical case studies, including MHz-range GaN inverters and robotic applications, will demonstrate the effectiveness of these methods. Future directions such as Simultaneous Wireless Power and Data Transfer (SWPDT) will also be briefly discussed.

Schedule

Time	Content
13:30 - 14:30	Fundamentals of Wireless Power Transfer
14:30 - 15:10	Advanced Load-Independent WPT Design
15:10 - 15:30	Coffee break
15:30 - 16:30	AI-Driven WPT Design Frameworks
16:30 - 17:00	Case Studies and Future Perspectives

Tutorial 13

Optical Biotelemetry Systems: Basics and Advances for Wireless Data and Power Transmission in Biomedical Implants

Sunday, May 24, 2026 | 13:30 – 17:00 (Afternoon) | Location: 5H

Andrea De Marcellis
(***University of L'Aquila,taly***)

Guido Di Patrizio Stanchieri
(***University of L'Aquila, Italy***)

Abstract: This tutorial introduces to the design of wireless communication systems for biomedical implants by making a detailed focus on the basics and advances of the optical biotelemetry. In particular, the design of new architectures of biomedical systems is demanding to fulfill the need to acquire and process biological/neural signals providing high-quality healthcare to sick people. Therefore, the following key-points are required: design of novel biomedical apparatus for prosthetic devices, diagnostic and therapeutic instrumentations, neural systems, etc., as well as guaranteeing the capability to transmit-receive data from inside and outside of the human body by means of high-efficiency implantable wireless data link solutions. Therefore, it is needed to develop implantable (transcutaneous) wireless biotelemetry systems achieving high data rate transmission, high efficiency characteristics (low-voltage/low-power), small Si area and low Bit Error Ratio.

Schedule

Time	Content
13:30 - 14:00	Introduction to the biotelemetry
14:00 - 14:30	Wireless data link systems: an overview and the State-of-the-Art
14:30 - 15:10	Optical wireless biotelemetry system design: analog/digital CMOS electronic circuits
15:10 - 15:30	Coffee break
15:30 - 16:10	Integrated photodetectors: Si photodiodes in CMOS technology
16:10 - 17:00	Optical wireless data and power transfer systems for implants: design and implementation

Tutorial 14

Leveraging IEEE DataPort and IEEE Data Descriptions for Enhanced Research Impact and Student Engagement

Sunday, May 24, 2026 | 13:30 – 17:00 (Afternoon) | Location: 5J

Yongfu Li
(***Shanghai Jiao Tong University, China***)

Qing Zhang
(***Shanghai Jiao Tong University, China***)

Abstract: This tutorial will provide an in-depth exploration of IEEE DataPort and IEEE Data Descriptions, emphasizing how to open-source datasets and write impactful academic papers. Additionally, we will discuss strategies for organizing and leveraging IEEE CAS Student Design Competitions to increase the visibility of research through the IEEE community. By attending, participants will learn how to enhance their work's discoverability, impact, and citation potential while engaging students in research competitions.

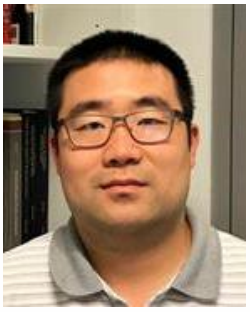
Schedule

Time	Content
13:30 - 14:00	Introduction to IEEE DataPort
14:00 - 15:10	IEEE Data Descriptions and writing impactful papers
15:10 - 15:30	Coffee break
15:30 - 16:40	Organizing IEEE CAS Student Design Competitions
16:40 - 17:00	Q&A and brainstorming session

Tutorial 15

Modern Power Amplifier Design: From Classical Principles to AI-Assisted Optimization

Sunday, May 24, 2026 | 13:30 – 17:00 (Afternoon) | Location: 5A



Xi Forest Zhu
(***University of Technology Sydney, Ultimo, Australia***)

Lang Chen
(***Sydnicon RF Microelectronics, Suzhou, China***)

Abstract: Modern wireless and sensing systems demand power amplifiers (PAs) that perform efficiently across an ever-widening frequency range, from sub-GHz to sub-THz. Designing PAs over such diverse regimes is challenging: designers must balance efficiency, linearity, and integration constraints, all of which vary with the semiconductor platform. CMOS, SOI, SiGe, and III-V technologies each bring different strengths and limitations, influencing achievable performance, power handling, and manufacturability.

This tutorial walks through PA design from fundamentals to advanced techniques. We start with classical PA architectures and key performance metrics at lower frequencies, then move to millimeter-wave and sub-terahertz designs, discussing power-combining methods, Doherty-inspired architectures, parasitic effects, and layout considerations. Process-specific trade-offs are highlighted, illustrated with real-world case studies that show how design choices impact performance across different technologies and frequency bands.

Finally, we look ahead to emerging trends and challenges in PA design, including integration, scalability, and design automation. By the end of the session, participants will have a clear understanding of the frequency- and process-dependent trade-offs that define modern PA design and practical guidance for building efficient, high-performance amplifiers for next-generation wireless and sensing systems.

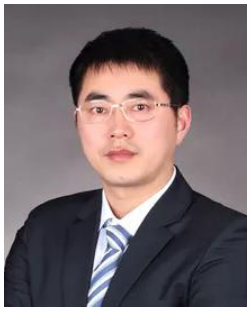
Schedule

Time	Content
13:30 - 13:50	Introduction to PA Fundamentals
13:50 - 14:30	Power Combining Techniques for PAs
14:30 - 15:10	Efficiency Enhancement Techniques for PAs
15:10 - 15:30	Coffee break
15:30 - 16:30	Case Studies: practical PA implementations across technologies
16:30 - 17:00	Discussion and Q&A on emerging trends and future challenges

Tutorial 17

Efficient Learning-based Models for Multimodal Data Compression

Sunday, May 24, 2026 | 13:30 – 17:00 (Afternoon) | Location: 5B+5C



Li Song (***Shanghai Jiao Tong University, China***)

Chuanmin Jia (***Peking University, China***)

Zhengxue Cheng (***Shanghai Jiao Tong University, China***)

Abstract: This tutorial surveys recent advances in learning-based data compression, focusing on achieving high performance with low computational complexity. While neural compression now rivals traditional codecs, its computational cost remains a barrier to practical deployment. This tutorial is structured into two interconnected parts to address this challenge. The first part establishes a foundational understanding of state-of-the-art learned compression for images and video. Then we'll explore efficient strategies including: (1) linear attention models (Mamba, RWKV) as alternatives of transformer and convolutions; (2) knowledge distillation for compact models; and (3) integrated restoration techniques for enhanced rate-distortion performance. The second part extends these principles to diverse modalities, covering sequential data (text, speech, tactile), multi-view representations (Gaussian Splatting, NeRF), and joint frameworks that share coding tools across data types to enable hardware savings. We conclude with key challenges and future directions for multimodal data handling and lightweight architectures.

Schedule

Time	Content
13:30 - 15:10	Comprehensive review and efficient compression models for image/video data
15:10 - 15:30	Coffee break
15:30 - 17:00	Extension to diverse data modalities in compression

Workshop Session

IEEE CAS Standards Workshop

The 5th Jointed Workshop between IEEE Standards Association and IEEE CAS - Secure Circuits and Systems: Standards for AI, Chiplets, and Healthcare

Date/Time: Sunday, 24 May 2026, 08:30–18:00

Location: 3A, SHICC, Level 3

As artificial intelligence, chiplet architectures, and next-generation healthcare technologies redefine the hardware landscape, secure and interoperable design remains paramount. The IEEE Circuits and Systems Standards Workshop—commemorating the 5th IEEE SA and IEEE CAS collaboration on standards, convened alongside ISCAS2026—invites professionals and researchers to engage with IEEE SA experts, industry innovators, and Working Group chairs. Participants will gain authoritative insights on IEEE standards for hardware security, healthcare electronics, and advanced circuits, while exploring secure, interoperable frameworks for AI and chiplet-based systems. This forum fosters strategic collaboration across academia, industry, and standards organizations. Register today to contribute to standards-driven innovation and connect with pioneers shaping the future of circuits and systems.

Technical Program

Time	Content
08:30-09:00	Registration & Welcome Coffee
09:00-09:10	Opening Remarks
09:10-10:00	IEEE SA: Standardization Driven Technologies
10:00-10:30	Updates for P3468: Standard for Chiplet Interface Circuit
10:30-10:50	Break
10:50-11:30	WG updates, SG updates
11:30-12:10	Panelist: Bridging the Gap: Turning CAS Research into IEEE SA Standards
12:10-14:00	Lunch
14:00-14:50	Minimally invasive implantable flexible BCI sensors and medical applications
14:50-15:40	Energy-Efficient mixed-signal designs for implantable devices
15:40-16:00	Break
16:00-16:30	Brain-computer interface assisted visual restoration
16:30-17:00	Call for participating: Wearable Implantable ExG Interface Circuits WG
17:00-18:00	Panelist discussion

CASS-CONNECT: Connecting Academia and Industry Workshop

Date/Time: Sunday, 24 May 2026, 13:30–16:30
Location: 3B, SHICC, Level 3

CASS-CONNECT is a new workshop at ISCAS 2026 designed to strengthen academia-industry collaboration across the IEEE CASS community. Building on the strong industry engagement demonstrated in recent CASS activities, the workshop will bring together leading researchers, industry practitioners and innovators to explore forward-looking technologies in circuits and systems. Key themes include high-performance processor design, energy-efficient AI hardware, healthcare technologies and diagnostics, as well as advanced sensing and signal processing.

The workshop will feature a series of talks from both industry and academia, complemented by interactive discussions and audience participation. These sessions aim to identify key challenges, align research and industrial priorities, and translate ideas into actionable recommendations and a roadmap for future collaboration. The workshop will also help seed a pipeline of potential partnerships and follow-on activities within the CASS community.

Attendance

Attendance is free, but capacity is limited. To request a place, please contact Professor Andreas Demosthenous at a.demosthenous@ucl.ac.uk with the subject line “CASS-CONNECT attendance request”.

Organizers

- Professor Andreas Demosthenous (University College London, UK)
- Emeritus Professor Izzet Kale (University of Westminster, UK)

Artificial Intelligence Workshop: Foundation Models, Compute Platforms, and Emerging Application

Date/Time: Monday, 25 May 2026, 15:00–17:30

Location: 5J, SHICC, Level 5

Dr. Don Tan

Vice President of IEEE Technical Activities; Chair of the IEEE Technical Activities Board; member of the National Academy of Engineering; IEEE Fellow

Topic: Data Center Challenges: Powering "the AI Factories"

Abstract: Recent studies predict the power level per rack in data centers is going from 100kW to 1MW (Microsoft, Google, and Meta). The overall electricity demand for "AI factories" is doubling to 1,000 TWh annually by 2030 (EPRI and Delloitte). "The end of AI is energy" sentiment reflects the severity of the "Power Wall" challenge (No conventional solutions). Breaking this seemingly-impossible "Power Wall" requires technical breakthroughs in the entire AI hardware/firmware ecosystems. Solution space includes, but not limited to, Liquid cooling from chip direct to plate, Immersion cooling with oil, Next-gen GPUs, TPUs and ASIC accelerators, HBM4 memories, WLP and specialized optical interconnects, Small modular nuclear reactors, Quantum computing and Fusion. Power connection/generation, distribution, processing and management are critical. Main events for powering computing industry are briefly reviewed, focusing on power, thermal management, and networking. Energy-efficient architecture are then discussed. Flexible electronic Large Power Transformers (FeLPTs) are emerging as a critical technology node. FeLPTs circuit options and challenges in interfacing with power grids are discussed. Structured microgrids, stand-alone or connected, are natural for efficient data center power parks. Desired features for UPS systems, together with its required storage capacity, are then presented. Potential in-rack, off-board, and on-board power processing circuits and system solutions are then explored.

Bio: Dr. Tan is a member of the National Academy of Engineering, a fellow of the IEEE and a PhD from Caltech. He has served as Distinguished Engineer, Fellow, Chief Engineer (Power Conversion), Program Manager, Senior Department Manager, and Center Director at a leading US Fortune 500 corporation. Unusually prolific as a visionary and impactful leader in ultra-efficient power conversion and electronic energy systems, Dr. Tan has pioneered breakthrough innovations with numerous high-impact industry firsts and record performances that received commendations from the highest level of the Government. He has developed hundreds of designs and thousands of hardware units deployed in high-impact space systems without a single on-orbit failure. His suite of world-class electronics performed flawlessly on the James Webb Space Telescope (JWST) one million miles away with world-record-breaking on-orbit technical performances, advancing humanity's understanding of deep space for years to come. Dr. Tan is IEEE Vice President and Technical Activities Board Chair in 2026. He has served as IEEE Transportation Electrification Council Founding President, IEEE Fellow Advisory/Oversight Subcommittee Chair, IEEE Industry Engagement Committee Vice Chair, Division II Director (IEEE Board of Directors), IEEE Fellow Committee Chair, IEEE PELS/PES eGrid Steering Committee Chair, PELS Long Range Planning Committee Chair, Nomination Committee Chair, PELS President, IEEE Journal of Emerging and Selected Topics in Power Electronics Founding Editor-in-Chief, APEC General Chair, PELS Vice President-Operations, Guest Editor-in-Chief for IEEE Transactions on Power Electronics and IEEE Transactions on Industry Applications, PELS Fellow Committee, PELS Vice President-Meetings, IEEE/Google Little Box Challenge Co-Chair, and IEEE/DoD Working Group Chair. Don has delivered more than 140 global keynotes and invited presentations. He has received more than $30M customer funding for research and technology. He serves on prestigious national and international awards and review or selection committees.

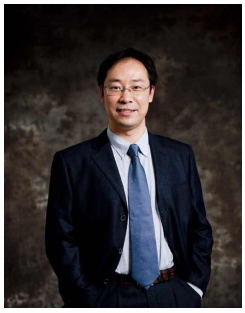
Prof. Hongxia Yang

Associate Dean of the Faculty of Computing and Mathematical Sciences and Executive Director of the PolyU Academy for AI, Hong Kong Polytechnic University

Topic: Co-GenAI: A Novel Fusion-Driven Framework

Abstract: We introduce a new framework that makes foundation model development more efficient, accessible, and collaborative. At its core is Domain-Adaptive Continual Pretraining (DACP), which combines lightweight efficiency via the first end-to-end FP8 low-bit training suite with collaborative expertise, embedding professional intuition through domain-specific models. DACP continuously adapts Large Language Models with unlabeled domain data, achieving superior specialization in underrepresented fields such as healthcare and science, while reducing GPU costs and outperforming mainstream systems. The framework also features an Advanced Model Fusion module. By integrating top-performing domain models regardless of their pretraining architecture, it constructs powerful foundation models in just 160 GPU hours, compared to the million-plus hours typically needed from scratch. Its Resource-Efficient Architecture further democratizes AI by enabling effective use of distributed, entry-level GPU clusters, lessening reliance on centralized compute. We also establish the first theoretical scaling law of model merging, providing a new principle for distributed generative AI. Real-world applications demonstrate its impact, with medical models surpassing Google MedGemma and multi-agent systems rivaling OpenAI's Deep Research. This framework reimagines foundation model development faster, cheaper, and more inclusive.

Bio: Prof. Hongxia Yang, Associate Dean of the Faculty of Computing and Mathematical Sciences and Executive Director of the PolyU Academy for AI (PAAI), is a Professor at The Hong Kong Polytechnic University. She received her PhD from Duke University, has published over 150 papers in leading conferences and journals, and holds more than 50 patents. She has received numerous prestigious awards, including the highest honor of the 2019 World Artificial Intelligence Conference (WAIC) - the Super AI Leader (SAIL) Award, the Second Prize of the 2020 National Science and Technology Progress Award, the First Prize of the Chinese Institute of Electronics Science and Technology Progress Award in 2021, and both the Forbes China Top 50 Women in Science and Technology and the Ministry of Education Science and Technology Progress Award (First Class) in 2022. Since 2023, she has been recognized as an AI 2000 Most Influential Scholar and was named one of the Top 50 Women in AI worldwide by CoinDesk, as well as a WAIC SAIL Top 30 Projects honoree in 2025. Her professional experience spans leading roles across academia and industry: she served as Head of LLM in the US at ByteDance, AI Scientist and Director at Alibaba Group, Principal Data Scientist at Yahoo! Inc., and Research Staff Member at the IBM T.J. Watson Research Center. She has also held joint adjunct professorships at Zhejiang University and the Shanghai Advanced Research Institute. Notably, she founded the foundation model teams at both Alibaba and ByteDance, establishing herself as a pioneer in the field of Generative AI.



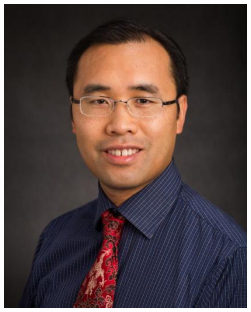
Prof. Yungang Bao

Professor and Deputy Director, Institute of Computing Technology, Chinese Academy of Sciences

Topic: Agile Development Practices for Open-source High-performance RISC-V Core - XiangShan

Abstract: In recent years, open RISC-V has led the trend in open-source processor design. XiangShan is an open-source high-performance RISC-V processor core that has become the highest-performing and most active open-source chip project internationally. It has been integrated into mass-production chips by multiple enterprises, achieving the industry's first product-level delivery and large-scale application of an open-source high-performance processor. This talk primarily discusses practical experiences from XiangShan's evolutionary journey, introduces various challenges faced during its agile development process and the corresponding solutions, and will also explore a series of unresolved open issues.

Bio: Yungang Bao is a professor of Institute of Computing Technology (ICT), Chinese Academy of Sciences (CAS) and the deputy director of ICT, CAS. Prof. Bao co-founded Beijing Institute of Open Source Chip (BOSC). His research interests include computer architecture and computer systems. He is leading the XiangShan project, One Student One Chip (OSOC) Initiative etc. His work was published on top conferences and journals such as ASPLOS, Communication of the ACM, HPCA, ISCA, MICRO etc. and was selected to IEEE Micro Top Picks. He was the winner of RISC-V International Technical Leadership Award, CCF-Intel Young Faculty Award of the year for 2013 and the winner of CCF-IEEE CS Young Computer Scientist Award and China's National Lofty Honor for Youth under 40 of the year for 2019.



Prof. Tao Xie

Peking University Chair Professor; Dean of Institute of Systems for Advanced Computing at Fudan University; Chief Scientist of Beijing Institute of Open Source Chip

Topic: RISC-V+AI OS: An Initiative of Building Foundations for Open and Trustworthy AI

Abstract:

Bio: Tao Xie is a Peking University Chair Professor, Dean of Institute of Systems for Advanced Computing at Fudan University (FiSAC), Chair of the Department of Software Science and Engineering in the School of Computer Science at Peking University, Chairman and Director of Beijing Tongming Lake Information Technology Application Innovation Center (TLAIC), Dean of Shanghai Institute of Systems for Open Computing (iSOC), Secretary General of Shanghai Open Processor Innovation Center (SOPIC), and Chief Scientist of Beijing Institute of Open Source Chip (BOSC). He was a Full Professor at the Department of Computer Science, the University of Illinois at Urbana-Champaign (UIUC), USA. He is a Foreign Member of Academia Europaea, and a Fellow of ACM, IEEE, AAAS, Chinese Institute of Electronics (CIE), and China Computer Federation (CCF). He won all three senior awards of ACM SIGSOFT (Outstanding Research Award, Influential Educator Award, Distinguished Service Award) etc. He serves as Director of CCF Technical Committee of System Software (TCSS). His main research interests include software engineering, system software, software security, trustworthy AI, RISC-V software ecosystem.

Prof. Jun Zhou

Professor at the University of Electronic Science and Technology of China; ultra-low-power AI processor design for intelligent sensing at edge

Topic: Ultra-Low-Power AI Processor Design for Intelligent Sensing at Edge

Abstract: Edge AI applications necessitate the integration of AI processors into smart devices that demand ultra-low power consumption and miniaturization. However, current commercial edge AI processors cannot meet the ultra-low-power AI computing needs of next-generation smart devices. Through algorithm-hardware co-optimization, the design of domain-specific edge AI processors can substantially reduce the power consumption of AI computation, while maintaining high accuracy and low cost with certain application flexibility. This talk discusses the design methodologies for ultra-low-power AI processors for edge scenarios, along with representative application cases.

Bio: Jun Zhou has been a Professor at the University of Electronic Science and Technology of China (UESTC) since 2017. Before joining UESTC, he worked at IMEC (the Netherlands) and the Institute of Microelectronics Singapore as a research scientist for around 10 years. He is a Council Member of the National Engineering Research Center for Advanced Microprocessor Technology, Director of the Embedded Artificial Intelligence Committee of Sichuan Institute of Electronics, and Deputy Director of Sichuan Engineering Research Center for Intelligent Circuits and Systems of Unmanned Systems. His research interests focus on ultra-low-power AI processor design for intelligent sensing at edge. He has published more than 150 papers in prestigious conferences and journals, including ISSCC and JSSC. He has designed and taped out a series of ultra-low-power AI processors for intelligent sensing applications including visual sensing, acoustic sensing, and smart wearables, achieving the lowest power consumption among the state-of-the-art designs while ensuring accuracy and real-time performance. He serves or has served as a member of the Digital Architectures and Systems (DAS) Subcommittee of ISSCC, Chair of the Digital Circuits and Systems (DCS) Subcommittee of A-SSCC, and Associate or Guest Editor of prestigious journals including JSSC, TBioCAS and TVLSI.

Workshop of the Cryo-Electronics for Quantum Systems and HPC (Cryo4QHPC) Special Interest Group

Date/Time: Sunday, 24 May 2026, 14:00–17:00

Location: 3D, SHICC, Level 3

Organizing Committee

Yong Lian, York University, Canada
Eduard Alarcon, UPC BarcelonaTech, Spain
Elena Blokhina, University College Dublin, Ireland
Wei Mao, Xidian University, Xi'an, China
Yongfu Li, Shanghai Jiao Tong University, Shanghai, China
Yanshu Guo, Shanghai Jiao Tong University, Shanghai, China
Yuxuan Luo, Zhejiang University, Hangzhou, China
Yan Liu, Shanghai Jiao Tong University, Shanghai, China

Technical Program

Time	Content	
09:00–09:10	Welcome and Opening Speech	Prof. Yong Lian
09:10–09:50	Invited Talk #1: Exploring the Noise Limit of Cryogenic Silicon Reflectometry for Quantum State Discrimination	Prof. Cheng Wang University of Electronic Science and Technology
09:50–10:30	Invited Talk #2: Cryogenic CMOS – From Device Level Physics to Reliable Cryogenic IC Design	Prof. Xufeng Kou ShanghaiTech University
10:30–10:40	Break	
10:40–11:20	Invited Talk #3: Energy-Efficient eDRAM-Based Cryogenic In-Memory Computing Accelerator	Prof. Yuhao Shu Nanjing University of Aeronautics and Astronautics
11:20–12:00	Invited Talk #4: Process Development of Low Temperature CMOS Technology for Low Temperature Digital And Analog Applications	Prof. Ran Cheng Zhejiang University
12:00–14:00	Lunch	
14:00–14:10	Opening	Prof. Eduard Alarcon
14:10–14:50	Invited Talk #5: Scientific talk Challenges and opportunities for development of ultra-low power scaled quantum computing systems	Sudipto Chakraborty IBM Research, US
14:50–15:30	Invited Talk #6: Milestones and Challenges in Cryo-CMOS for Quantum Computing & Next steps for the SIG	Prof. Elena Blokhina University College Dublin
15:30–15:40	Break	
15:40–16:20	Invited Talk #7: CO-LINK: Cryogenic Optical Link for Cryogenic High-Performance Computing and Scalable Quantum Computing	Prof. Hanjun Jiang Tsinghua University
16:20–17:00	Invited Talk #8: Young Professional talk	Pau Escofet Universitat Politècnica de Catalunya
17:00–17:40	SiG Cryo4QHPC Officers' Election	

INVITED SPEAKER #1

Prof. Cheng Wang

Professor, School of Electronic Science and Engineering, University of Electronic Science and Technology, Chengdu, China

Topic: Exploring the Noise Limit of Cryogenic Silicon Reflectometry for Quantum State Discrimination

Abstract: Quantum state discrimination dominates the cycle of quantum error correction. The fidelity and integration time are limited by the noise temperature of RF reflectometers. This talk introduces the recent progress of ultra-low noise cryogenic CMOS readout circuits from integrated physics group (IPG) in UESTC, including 4 aspects: gm-boosting low noise amplifier (LNA), noise canceling LNA, degenerated parametric amplifier (DPA) and mixer-first reflectometer. All of these works have achieved the state-of-the-art noise performance, pushing the boundary of quantum state readout.

Bio: Cheng Wang, Professor, School of Electronic Science and Engineering, University of Electronic Science and Technology (UESTC). He received the B.E. degree from Tsinghua University in 2008, and the Ph.D. degree from Massachusetts Institute of Technology (MIT) in 2020. His research spans from cryogenic circuits for quantum sensing and control, molecular spectroscopy & clock, and terahertz phased array. He has received a series of awards such as the 2024 Sichuan Youth May Fourth Medal, the recognition as “35 innovators under 35” (China) by the MIT Technology, the IEEE Solid-State Circuit Society (SSCS) Predoctoral Achievement Award, the MIT Microsystem Technology Laboratory (MTL) Doctoral Dissertation Seminar Award, the Chinese Government Award for Outstanding Self-Financed Student Abroad. As the chairman of the technical committee (TPC chair), he hosted the IEEE IMWS-AMP 2023 and RFIT 2024 international conferences.

INVITED SPEAKER #2

Prof. Xufeng Kou

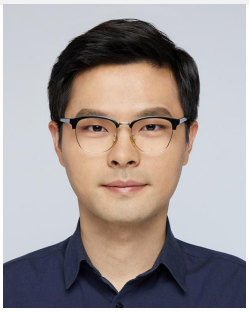
Professor and Executive Dean, School of Information Science and Technology, ShanghaiTech University, Shanghai, China

Topic: Cryogenic CMOS – From Device Level Physics to Reliable Cryogenic IC Design

Abstract: Cryogenic CMOS (Cryo-CMOS) technology has emerged as a key paradigm to bypass the power and memory-wall bottlenecks in advanced semiconductor scaling, enabling steep subthreshold swings and minimized leakage currents. Nevertheless, complex physical phenomena such as dopant freeze-out and band-tail effects cause severe extrapolation inaccuracies and numerical instabilities in standard commercial compact models, thereby blocking robust cryogenic IC design. To resolve these bottlenecks, this talk proposes a generic, continuous compact modeling scheme calibrated from 300 K down to 4.2 K, and demonstrates its application in cryogenic-optimized device and circuit design.

Bio: Dr. Xufeng Kou is a Professor and Executive Dean of the School of Information Science and Technology at ShanghaiTech University. He received his BS degree (with honor) in Chu Kochen Honors College from Zhejiang University (2009). From 2009 to 2015, he received his MS and PhD degrees in Electrical Engineering from UCLA. Since February 2016, he joined the School of Information Science and Technology at Shanghai Tech University. So far, Dr. Kou has published 3 book chapters, and co-authored more than 90 peer-reviewed journal/conference papers including Nature Electronics, Nature Materials, Nature Nanotechnology, Nature Communications, Physical Review Letters, and IEEE IEDM. with more than 7000 citations (h-index of 36). He also holds several awards including the Qualcomm Innovation Fellowship (2012), Chinese Outstanding Student Abroad Scholarship (2013), Distinguished PhD Dissertation Award of UCLA (2015), Shanghai May 4th Youth Medal (2018), Shanghai 35U35 Award (2021), and Shanghai Pudong Elite Researcher Award (2023).

INVITED SPEAKER #3



Prof. Yuhao Shu

Associate Professor, College of Integrated Circuits, Nanjing University of Aeronautics and Astronautics, China

Topic: Energy-Efficient eDRAM-Based Cryogenic In-Memory Computing Accelerator

Abstract: This talk presents our recent work on energy-efficient eDRAM-based cryogenic in-memory computing accelerators. Cryogenic CMOS provides opportunities to improve device and circuit behavior, while cooling overhead in cryogenic systems makes energy efficiency an important design objective. The talk first introduces an eDRAM-based cryogenic IMC accelerator that supports multiple operation modes through cryogenic-aware bitcell and readout schemes. It then discusses an extension toward multi-bit eDRAM-based analog cryogenic IMC for higher computing density. Together, these designs highlight the potential of eDRAM-based cryogenic IMC as an energy-efficient computing platform for data-intensive workloads.

Bio: Yuhao Shu (Member, IEEE) is an Associate Professor at the College of Integrated Circuits, Nanjing University of Aeronautics and Astronautics, China. His research interests include cryogenic CMOS circuits, in-memory computing, and energy-efficient circuit and system design. He has completed more than 10 chip tape-outs and published 13 first-/corresponding-author papers in journals and conferences including IEEE JSSC, TCAS-I, and CICC.

INVITED SPEAKER #4

Prof. Ran Cheng

Associate Professor, College of Integrated Circuits, Zhejiang University, Hangzhou, China

Topic:Process Development of Low Temperature CMOS Technology for Low Temperature Digital And Analog Applications

Abstract: In this work, we report DTCO-assisted process development of low-temperature (LT) CMOS technology on a standard 55-nm foundry platform, spanning process engineering, library validation, processor-level evaluation, and reliability analysis. Methods for threshold-voltage (VT) modulation were evaluated among various CMOS platforms. For 55 nm process, doping engineering was implement, enabling improved device electrostatics at 77 K. Based on wafer-level characterization and device models, a dedicated LT PDK and corresponding standard cell libraries are developed and experimentally validated. Improvement of logic gates delay and processor level power efficiency at 77 K were demonstrated. Variability and hot carrier issues were also discussed to complement the device-level study. The reported VT modulation methodology establishes a practical route for realizing balanced PPAC of LT CMOS for high-speed and energy-efficient computing.

Bio: Dr. Ran Cheng received her B.Eng. (Hons) and Ph.D. degrees in Electrical and Computer Engineering from the National University of Singapore, Singapore. She is currently an Associate Professor with the College of Integrated Circuits, Zhejiang University, Hangzhou, China. Dr. Cheng's research includes cryogenic CMOS, emerging memory, and logic-memory joint applications. She has published over 80 peer-reviewed papers in the relevant fields, and is leading several major research projects on low temperature CMOS and ferroelectric circuits supported by national and provincial funding agencies.

INVITED SPEAKER #5

Prof. Sudipto Chakraborty

IBM Research, US

Topic: Scientific talk Challenges and opportunities for development of ultra-low power scaled quantum computing systems

Abstract:

Bio: Sudipto Chakraborty (B. Tech, IIT, Kharagpur, 1998, Ph.D from GaTech, 2002) was with Texas Instruments till 2016 where he designed low power IC for >10 product families in automotive/wireless/medical/microcontrollers. Since 2017 he led the low power circuit design for next generation quantum computing applications in IBM research using nanometer CMOS. He has authored or co-authored >90 papers, two books and 95 US patents. He has served in the TPC including ISSCC, CICC, RFIC, IMS, and is an IBM master inventor. He serves as an associate editor of TCAS-I, TCAS-II, CASS magazine and distinguished lecturer in the IEEE MTT-S, CASS and SSCS.

INVITED SPEAKER #6

Prof. Elena Blokhina

Associate Professor, University College Dublin

Topic: Milestones and Challenges in Cryo-CMOS for Quantum Computing & Next steps for the SIG

Abstract:

Bio: Elena Blokhina received the Habilitation à Diriger des Recherches (HDR, equivalent to DSc) in Electronic Engineering from Sorbonne Université, as well as a PhD in Physical and Mathematical Sciences and an MSc in Physics with highest honours from Saratov State University. Since 2007, she has been with University College Dublin, where she is currently an Associate Professor. She is a member of the Institute of Physics, a Senior Member of IEEE and has held several leadership roles within the IEEE Circuits and Systems Society and the IEEE Microwave Theory and Technology Society, including serving on the IEEE Circuits and Systems Society Board of Governors. Prof. Blokhina has chaired and organised numerous international conferences and workshops in physics, electronics, semiconductor technologies and quantum computing, including events associated with IEEE ISCAS, IEEE ICECS and ESSERC. She previously served as Associate Editor and later Deputy Editor-in-Chief of IEEE Transactions on Circuits and Systems I, Her research focuses on quantum computing, quantum information processing, quantum electronics, and on-chip classical and quantum information processing. Elena Blokhina received the Habilitation à Diriger des Recherches (HDR, equivalent to DSc) in Electronic Engineering from Sorbonne Université, as well as a PhD in Physical and Mathematical Sciences and an MSc in Physics with highest honours from Saratov State University. Since 2007, she has been with University College Dublin, where she is currently an Associate Professor. She is a member of the Institute of Physics, a Senior Member of IEEE and has held several leadership roles within the IEEE Circuits and Systems Society and the IEEE Microwave Theory and Technology Society, including serving on the IEEE Circuits and Systems Society Board of Governors. Prof. Blokhina has chaired and organised numerous international conferences and workshops in physics, electronics, semiconductor technologies and quantum computing, including events associated with IEEE ISCAS, IEEE ICECS and ESSERC. She previously served as Associate Editor and later Deputy Editor-in-Chief of IEEE Transactions on Circuits and Systems I, Her research focuses on quantum computing, quantum information processing, quantum electronics, and on-chip classical and quantum information processing..

INVITED SPEAKER #7

Prof. Hanjun Jiang

Professor and Vice Dean, School of Integrated Circuits, Tsinghua University, Beijing, China

Topic: CO-LINK: Cryogenic Optical Link for Cryogenic High Performance Computing and Scalable Quantum Computing

Abstract: The cryogenic high performance computing (HPC) is attracting substantial interests due to the promising performance of integrated circuit under low temperature and also the consideration of critical cooling requirement with increasing computing power consumption. The scalable quantum computing application is another important scenario for cryogenic electronics. Both applications require high-bandwidth data link working in the cryogenic environment, and also the data link across different temperature domains. This talk briefly review the possible solutions for cryogenic data link for these applications, and then focus on the cryogenic optical data link technique. A 56 Gbps cryogenic optical data link design will be shown as a demonstration of this technique. The link architecture, data transceiving ASICs and the preliminary experimental results will be presented.

Bio: Hanjun Jiang received the B.S. degree in electronic engineering from Tsinghua University, Beijing, China, in 2001, and the Ph.D. degree in electrical engineering from Iowa State University, Ames, IA, USA, in 2005. From 2005 to 2006, he was with Texas Instruments, Dallas, USA. He has been with the School of Integrated Circuits (formerly the Institute of Microelectronics), Tsinghua University since 2007, where he is currently a full professor and the vice dean. His current research interest mainly focuses in the area of low power integrated circuits and systems for the emerging applications including the biomedical micro-systems, quantum computing, etc. He has authored and co-authored over 200 peer-reviewed journal and conference papers, and contributed to 3 books. He holds more than 40 patents. He was the IEEE Solid-State Circuits Society Beijing Chapter Chair from 2015 to 2018, an associate editor of TBioCAS from 2016-2025 and TCAS-II from 2022 to 2023, and IEEE Distinguished Lecturer for the term of 2024-2025. He now serves as an associate editor of IEEE OJ-SSCS.

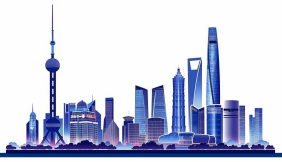
INVITED SPEAKER #8

Prof. Pau Escofet

Topic: TBD

Bio: Pau Escofet is a PhD student specializing in Quantum Computing Architecture at the N3Cat group at Universitat Politècnica de Catalunya (UPC). He earned his Bachelor's Degree in Computer Science from UPC in 2022, during which he completed an exchange semester at ETH Zurich. Pau continued his academic journey at UPC, obtaining a Master's Degree in Advanced Telecommunication Technologies in 2023. His PhD research focuses on scalable architectures for quantum computing, specifically targeting systems that can support thousands or millions of qubits to achieve quantum advantage.

Throughout his academic career, Pau has been recognized for his outstanding achievements. In 2021, he received the award for the Best Computer Science Bachelor's Thesis for his work on "Spectral Methods for Graph Drawing and Synthesis of Integrated Circuits" from FIB Alumni. He was also honored as one of the Top 10 Computer Science students in Spain in 2022 by Nova Talent's Nova 111 Student List. Additionally, his exceptional work in high school earned him the Best Chemistry High-School Thesis award from Universitat Ramon Llull in 2018.



IEEE CASS Chapter Leadership Workshop

Date/Time: Tuesday, 26 May 2026, 14:00-17:30

Location: 5I, SHICC, Level 5

Organizers

- Xinfei Guo, AEiC of IEEE TVLSI, Shanghai Jiao Tong University
- Chao Wang, Wuhan CASS Chapter Chair, Huazhong University of Science and Technology
- Taniguchi Ittetsu, IEEE CASS BoG (R10 MaL), The University of Osaka
- Yongfu Li, IEEE CASS VP RAM, Shanghai Jiao Tong University

Agenda

Time	Content	
14:00-14:10	Opening Remarks & Workshop Objectives	IEEE CASS Leader
14:10-14:40	IEEE CASS Global Chapters	Yongfu Li, IEEE CASS Vice President, RAM
14:40-15:00	Awardee Presentations & Lightning Q&A Part I (2 Speakers)	• IEEE Egypt CASS Chapter Sharing by Prof. Ahmed H. Madian • IEEE Chile CASS Chapter Sharing by Prof. Jorge Marin
15:00-15:20	Short Break	
15:20-16:10	Awardee Presentations & Lightning Q&A Part II (5 Speakers)	• IEEE Sri Lanka CASS Chapter Sharing by Prof. Chamira U. S. Edussooriya • IEEE Islamabad (Pakistan) CASS Chapter Sharing by Prof. Nosherwan Shoaib • IEEE CASS Kenya Chapter Sharing by Prof. Shadrack Mambo • IEEE Hyderabad (India) CASS Chapter Sharing by Prof. J. V. R. Ravindra • IEEE Bangalore (India) CASS Chapter Sharing by Prof. Aloke Kumar Das
16:10-17:30	Benchmark Activities	

WiCAS-YPCAS Event

Date/Time: Monday May 25, 2026, 18:00-21:30

Location: Europe Hall, SHICC, Level 5

Time	Content
18:00-18:10	Welcome and Opening Speech
18:10-18:30	Invited Talk #1: Sustainable Impact: Building an Inclusive Global Career in Clean Energy & Technology Leadership
18:30-18:50	Invited Talk #2: The Road Back: What Industry Experience Taught Me About Becoming Faculty
19:00-19:20	Panel discussion student mentoring discussion
19:20-19:30	Student Q&A followed by open discussion with mentors
19:30-21:30	Free networking and dinner

Talk Title: "Sustainable Impact: Building an Inclusive Global Career in Clean Energy & Technology Leadership"

Abstract

The global energy transition requires not only technical innovation, but also inclusive leadership, cross-sector collaboration, and purpose-driven career pathways. In this talk, Simay Akar Koehler shares her journey from engineering and global solar manufacturing to executive leadership, entrepreneurship, and international volunteer governance within IEEE.

Through the lens of IEEE Women in Engineering (WIE) and global volunteer leadership, she will explore how diversity, representation, and mentorship accelerate both technological progress and career advancement. She will discuss how young professionals — especially women and underrepresented engineers and technologist — can intentionally design impactful careers in clean energy and emerging technologies, navigate cross-border opportunities, and integrate sustainability, equity, and systems thinking into their professional growth.

Drawing from her experience in industry and IEEE leadership, the session will highlight the power of professional communities such as WIE in creating visibility, sponsorship, and global networks that enable inclusive innovation. The goal is to empower students and early-career engineers to see themselves not only as technologists, but as global change agents shaping a more sustainable and equitable future.

Brief Biography

Simay Akar Koehler

Founder & CEO | AKEC Sustainable & Greentech Solutions

Board Member & Co-Founder | Innoses

Simay Akar Koehler is a globally recognized, multi-award-winning sustainable energy executive, serial entrepreneur, and mission-driven systems strategist with deep expertise in climate solutions, inclusive innovation, and environmental justice.

She is the Founder and CEO of AKEC Sustainable & Greentech Solutions, a purpose-driven advisory firm advancing the global energy transition through strategic planning, technology evaluation, market expansion, and sustainable supply chain transformation for clean energy innovators and impact-focused enterprises.

She is also the Co-Founder and Board Member of Innoses, a vertically integrated battery energy storage company, where she previously served as Chief Commercial Officer, leading global growth, financing strategies, and ecosystem partnerships to scale reliable and affordable clean energy technologies worldwide.

With extensive international experience across solar photovoltaics manufacturing, battery energy storage systems, electric mobility, and just energy transition programs, Simay bridges public-private partnerships, nonprofit impact, and responsible entrepreneurship. Her global footprint spans Türkiye, China, and the United States, with clean energy collaborations across more than 70 countries.

In addition to her executive career, she serves in several senior IEEE leadership roles, including:

- Vice President, Career & Member Services, IEEE-USA Board (2026)
- Treasurer, IEEE Humanitarian Technologies Board (2025–2026)
- Global Chair-Elect (2026); Chair (2027–2028), IEEE Women in Engineering Committee
- Chair, IEEE Central Indiana Section (2025–2026)

A Senior Member of IEEE and member of Eta Kappa Nu (HKN), she is a passionate advocate for women's leadership in climate and clean energy and mentors emerging leaders globally.

Website: https://www.simayakar.com/

Talk Title: The Road Back: What Industry Experience Taught Me About Becoming Faculty

Abstract

After completing my PhD, I spent several years in industry, working across three companies-Qualcomm, Intel, and Seagate. These experiences not only broadened my technical perspective but also shaped my long-term career aspirations, ultimately leading me back to academia. In this talk, I will reflect on my journey through industry and share key lessons that have influenced my approach to research, collaboration, and problem-solving. I will also discuss the challenges of transitioning into academia, as well as the evolving landscape of higher education and its impact on how we navigate academic careers today.

Brief Biography

Hai (Helen) Li

Marie Foote Reel E'46 Distinguished Professor and Department Chair

Electrical and Computer Engineering Department, Duke University

Hai (Helen) Li is the Marie Foote Reel E'46 Distinguished Professor and Department Chair of the Electrical and Computer Engineering Department at Duke University. She received her B.S. and M.S. degrees from Tsinghua University and her Ph.D. degree from Purdue University. Her research interests include neuromorphic circuits and systems for brain-inspired computing, machine learning acceleration and trustworthy AI, conventional and emerging memory design and architecture, and software and hardware co-design.

Dr. Li served/serves as the Associate Editor-in-Chief and Associate Editor for multiple IEEE and ACM journals. She was the General Chair or Technical Program Chair of multiple IEEE/ACM conferences and the Technical Program Committee member of over 30 international conference series.

Dr. Li has received many awards, including the IEEE Edward J. McCluskey Technical Achievement Award, Ten-Year Retrospective Influential Paper Award from ICCAD, TUM-IAS Hans Fischer Fellowship from Germany, ELATE Fellowship, nine best paper awards, and another ten best paper nominations from IEEE/ACM. Dr. Li is a fellow of IEEE, AAAS, ACM, and NAI.

Industry Forum I

Title: AI-Driven Innovation for the Future Chip Design

Tuesday , May 26, 2026 | 15:00 - 17:00 **Location: Grand Ballroom 1, SHICC, Level 7**

Dr. Chunyang Feng

VP of R&D, Giga Design Automation

Topic: Giga-da EDA Platform Enabling Heterogeneous Chip Design in the Post-Moore Era

Abstract: In the post-Moore era, as traditional process scaling approaches its physical limits, chip design paradigms are shifting toward heterogeneous integration (Chiplet, 3D-IC) and system-level co-innovation. Giga-da has broken through the bottlenecks of 3D-IC design with fully self-developed technologies, offering an end-to-end solution from system planning, physical implementation, to multi-physics signoff. This empowers AI accelerators, HBM memory, and other high-performance chips with domestically developed tools, supporting China's semiconductor industry in achieving technological autonomy and innovation breakthroughs in the post-Moore era.

Bio: Dr. Feng holds a Ph.D. in Microelectronics and Solid-State Electronics from Fudan University. Currently serving as Vice President of Shenzhen Giga Design Automation Co., Ltd., he leads the R&D of the digital sign-off tools and AI-related products.

Prior to joining Shenzhen Giga Design Automation, Dr. Feng worked at the R&D Center of Synopsys Shanghai, where he participated in the development of digital EDA tools for placement and routing, static timing analysis, and other key areas. He also served as a researcher at the Artificial Intelligence Research Center of Duke Kunshan University, bridging academic insights with practical applications. He has over 16 years of industry experience in the VLSI domain.

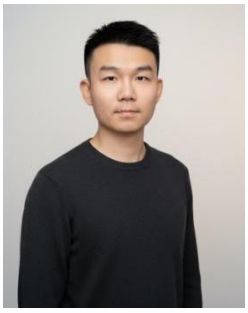
Dr. Alex Song

Head of IC R&D Operations, UNISOC

Topic: Thoughts in Edge AI design and the role of AI agentic in AI chip development

Abstract: The rapid evolution of AI in the recent years, motivates more and more fabless design companies to explore the edge AI chip design in the AI inference territory, and the market is predicted to be growing explosively in the next few years. As the industry leader in telecommunication, and the top fabless design company in China, UNISOC has unique strength and competitive edge designing Edge AI chips. Dr Song will focus on the power efficiency aspect of edge AI chip design, which cornerstones the core competitive advantage of the product. The quick adoption of AI agentic in the chip design flow has proved its value in terms of accelerating the design process, as well as improving the design quality. Dr Song will also discuss his understanding of the chemistry between AI agentic and design design flow, and the highlights of AI agentic practices in UNISOC.

Bio: Dr song is currently heading the IC R&D operation of UNISOC, responsible of designing a wide range of ASIC product from high performance mobile processors, IOT devices, and display TV socs etc. His prior experiences of more than 20 years in the industry also includes technical management positions at Hisilicon, ST microelectronics, and many other companies. Dr Song holds Ph.D. degree in microelectroics and solid-state from Fudan University.



Mr. Sze SiuFung-Keith

Senior Director of Software R&D, Ninenovo

Topic: AI for Preventive Wellness: Building the Next Generation of Wearable Health Intelligence

Abstract: This talk explores how AI can transform wearable health products from simple data trackers into proactive wellness intelligence systems. By understanding each user's personal health patterns, AI can help identify meaningful changes, explain what they may indicate, and provide practical micro-actions for daily improvement. The presentation will discuss how wearable devices and AI can work together to support preventive wellness, long-term behavior change, and a more personalized health experience.

Bio: Sze SiuFung-Keith serves as Senior Director of Software Research and Development.He has extensive professional experience in wearable technology, artificial intelligence, and the research and development of intelligent health products. He focuses on empowering consumer wearable devices with cutting-edge AI algorithms to enhance personal health management systems.

With in-depth insights into the full lifecycle development of wearable health intelligence products, Sze SiuFung-Keith has long been dedicated to exploring the integration of artificial intelligence with preventive wellness scenarios. He leads the technical team in iterating core health data analysis frameworks and is committed to building more accurate, personalized, and proactive intelligent health perception systems for end users.

Industry Forum II

Title: Charting the Next Era of Semiconductors

Tuesday , May 26, 2026 | 15:00 - 18:15 **Location: Yellow River, SHICC, Level 3**

Abstract

As semiconductor scaling approaches lithographic and fundamental atomic limits, the traditional paradigms of Moore's Law and Dennard's Law are losing their effectiveness. Without transistor shrinking as the primary lever, how can performance continue to scale?

This remains one of the industry's most critical open questions. In this forum, prominent local enterprises will present its latest architectural innovations and engineering practices in mobile SoCs and AI computing chips, followed by a panel discussion to explore a new sustainable scaling path for the next decade. We cordially invite you to join the conversation.

Schedule

Time	Content		Session chair
15:00-15:05	opening		Yong Lian, York University
15:05-15:45	Topic 1	Practices of SoC Design with Novel Architectures	Huang Yong, Huawei's fellow
15:45-16:25	Topic 2	Computing Chip Design:Engineering Choices and Trade-offs	Xia Jing Huawei's fellow
16:25-16:40	Coffee Break		
16:40-17:55	Panel discussion		Chair：Handel H. Jones & Heng Liao Six panelists
17:55-18:10	Q&A		
18:10-18:15	Session Closing		

IEEE CASS Student Design Competition

Event Overview

The IEEE CASS Student Design Competition provides student teams with an opportunity to present innovative circuit and system designs and compete at the world level during ISCAS 2026.

- Details: https://ieee-cas.org/society-involvement/student-design-competition
- Final Competition Time: 15:00-16:00, 2026-May-25th
- Final Competition Venue: Yangtze River Hall, SHICC, Level 5

Quick Stats

Region	Total Teams Registered to Participate in Phase One	Total Chapters Represented
R1-7	8	2
R8	55	7
R9	19	13
R10	61	10

Finalist Teams

Winning Teams who will compete in the World Level:

R1-7 Team "Team TacTile"	R8 Team "Hand Gesture Controller for human-machine interaction"
Members: • Avery Janenda • Amelia Pillar • Mina Schepmann • Tomi Kuye • Brian Mercado • Hannah Wixom	**Members:** • YanSheng Zhao • Yuhao Zhang • Yasim Thayyil • Ahmad Suleiman Muhamma • Yash Modha
R9 Team "Biomechanical Analysis System for Single-Plane Joint Range of Motion Using Computer Vision"	**R10 Team "Hardware-Efficient FSRCNN Accelerator"**
Members: • Mariana Camacho Orgaz • Jhoselin Heredia Ichota • Karen Flores Alvarez • Eynar Calle Viles	**Members:** • Junsik Lee • Jungho Lee • Suhwan Jo • Gwangseon Shin

IEEE CASS Mentoring Program

Date/Time: Monday, May 25, 2026, 16:00–17:00
Location: Yangtze River Hall, SHICC, Level 5

Overview

The IEEE CASS Mentoring and Networking Session is a dedicated one-hour event organised as part of the IEEE Circuits and Systems Society (CASS) Mentoring Program, co-organised with IEEE WiCAS-YP and supported by the UCL IEEE Student Branch. This session is designed to provide structured and inclusive mentoring opportunities for student attendees at ISCAS 2026. It connects undergraduate, Master's, and PhD students with experienced researchers and industry professionals from the circuits and systems community in an informal and supportive environment.

The programme combines small-group mentoring discussions with a guided Q&A, focusing on research directions, career development, and professional growth. It is particularly suitable for students who are:

- Exploring research and long-term career pathways
- Seeking perspectives on academic and industrial career options
- Attending ISCAS for the first time
- Interested in engaging more actively with IEEE CASS, WiCAS, and Young Professionals activities
- Participation is open to invited participants and applicants. Spaces are limited.

Call for Mentors

Academics and industry professionals within the circuits and systems community are warmly invited to participate as mentors.

Mentors will engage in small-group discussions, offering perspectives on research, career development, and professional growth. The expected time commitment is approximately one hour, and no formal preparation or presentations are required.

Prospective mentors are invited to contact the organising team with a short CV or a link to a professional webpage or profile. Mentors are encouraged to send the template slide.

Contact

Students and mentors wishing to participate or enquire further are invited to contact the organising team at yu.wu.09@ucl.ac.uk with email subject: **[ISCAS Mentoring].**

Additional Opportunity: WiCAS-YPCAS Event

All participants in the mentoring session will receive an invitation to attend a subsequent IEEE WiCAS-YPCAS Event during ISCAS 2026, featuring invited speakers, a panel discussion, and networking activities with senior members of the community.

Further details, please see the WiCAS-YPCAS Event webpage.

Organising Committee

- Yu Wu (University College London)
- Seerat Sekhon (University College London)
- Yongfu Li (Shanghai Jiao Tong University)
- Yoko Uwate (Tokushima University)
- Fakhrul Zaman Rokhani (Universiti Putra Malaysia)

Lecture Presentations (Oral)

Timing and Format

Duration: Each presentation slot is 15 minutes in total. This includes 12 minutes for the presentation itself and 3 minutes for questions from the audience (Q&A).

Slide Aspect Ratio: Please prepare your slides in 16:9 widescreen format for optimal display.

Technical Facilities

A high-definition LCD projector and a local PC (Windows 7, MS PowerPoint, and Adobe Acrobat Reader) will be available in every session room for regular presentations.

Preparation and Upload

Media: You must bring a USB memory stick containing your presentation file.

Compatibility: To avoid software compatibility problems (MS PowerPoint), speakers are advised to EMBED ALL FONTS in your PowerPoint file and bring a backup PDF version of your presentation.

Uploading: Files can be uploaded to the local PCs in the lecture rooms during the morning breaks, lunch breaks, or at least 15 minutes before the initial sessions start.

Reporting to Session Chair

Speakers should arrive in their assigned session room 15 minutes BEFORE the start of the session to report to the Session Chair. A volunteer will be available in the room in case you need assistance.

Lecture Session Schedule - Detailed Agenda

Modeling, Sensors, and Emerging Analog Systems Session

Session Code:	**A2L-01**	**Date & Time:**	**Monday May 25, 2026 (10:30 - 12:00)**
Location:	**3C**	**Chairs:**	**Filippo Neri, Nagendra Krishnapura**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1753	1.8	Compiled, Parasitic-Aware Mom Capacitor Arrays Experimentally Evaluated in SAR ADC *Shujia Sun, Zhao Gao, Xu Cheng, Xiaoyang Zeng*
2775	1.1	On Resistor Nonlinearity Modeling for Low-Distortion Analog Circuits *Nagendra Krishnapura, Paramita Banerjee, Bobba Bhavani, Yadala Venkat*
2351	1.4	A 15-Bit 22-μW 3.91-aF Power/Measurement-Time Scalable Direct Capacitance-to-Digital Converter with Closed-Loop Ratio-Based Floating Inverter Dynamic Amplifier *Ruixue Ding, Bo Zhao, Yuke Shen, Jiahe Li, Tao Chen, Yuanhao Zhao, Jiuhuan Feng, Yi Shen, Shubin Liu, Zhangming Zhu*
1902	1.8	A 94.3%-Efficient Battery-Less Wireless Sensor Node Featuring -0.5°C～+1°C Inaccuracy Room Temperature Two-Point Calibrated Sensor *Ju-Won Oh, Sung-Jae Lee, Jong Wan Jo, Yeon-Jae Jung, Young-Gun Pu, Kang-Yoon Lee, Jun-Eun Park*
2808	1.1	A Self-Built Continuous Temperature Compensation Circuit for Logarithmic Amplifier *Xinwei Yu, Zihao Xia, Siming Zhang, Bing Bai, Dongdong Chen*

High-Speed Data Converters and Time-Domain ADCs Session

Session Code:	**A2L-02**	**Date & Time:**	**Monday May 25, 2026 (10:30 - 12:00)**
Location:	**3I+3J**	**Chairs:**	**Tawfiq Musah, Luis Oliveira**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2862	1.3	A 5V Swing, 20GS/s, 6-Bit Current Steering DAC Utilizing LDMOS in 22nm FDSOI CMOS *Jendrik Kellermann, Urs Hecht, Philipp Nickel, Friedel Gerfers*
2557	1.3	A 10-Bit 6.4-GS/s Current Steering DAC with -163.7 dBm/Hz Noise Spectral Density for DPD-Based D-Band Backhaul Transmitters *Antonio Aprile, Edoardo Bonizzoni, Piero Malcovati*
1105	1.3	A 9-Bit 1.2GS/s Gain-Programmable Stochastic Time-to-Digital Converter with Sub-Ps Resolution *Shin-Hyun Jeong, Dongsoo Lee, Han-Kyoung Lee, Yong-Un Jeong Jeong, Woo-Seok Choi*
1110	1.3	A 97.63 fJ/Conv-Step 3 GSa/s 2-Way Time-Interleaved (Ti) 3-Bit Flash ADC for Analog In-Memory Computing (Imc) Deep Learning (DL) Accelerators in 28-nm CMOS *Jinhua Wang, Adam Slater, Travis Blalock, Steven Bowers*
1369	1.3	A 6-Bit 2.15-GS/s 1.05-mW Flash-Assisted Time-Domain ADC with 0.8-V Supply *Utkarsh Sharma, Behzad Razavi, Chih-Kong Ken Yang*

High-Speed Interface and Wireline Circuits Session

Session Code:	**A2L-03**	**Date & Time:**	**Monday May 25, 2026 (10:30 - 12:00)**
Location:	**3A**	**Chairs:**	**Navid Yazdi, Yanquan Luo**

Papers are listed in the order they will be presented.

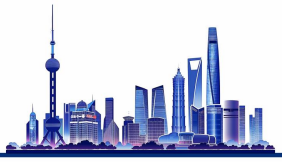
Paper Id	Topic	Title/Author
1387	1.4	A 4x106 Gb/s PAM4 Current-Reuse VCSEL Driver with a High-Bandwidth VGA in 130 nm BiCMOS *Wei Chen, Jiahao Chen, Minhao Li, Yuchen Liu, Ying Wu, Pisen Zhou, Patrick Yin Chiang, Ronghua Ni*
2096	1.4	A 1.2−3.4 Gb/s Low-Power Multiphase CDR with Glitch-Free Bang-Bang Phase Detector *Youngryul Yun, Min-Jeong Son, Do-Yeon Jeon, Ji-Seul Yoon, Seung-Jin Yeo, Jae-Hong Ko, Muhammad Abrar Akram, In-Chul Hwang*
2207	1.4	A 0.74 pJ/Bit 10 Gbps PAM-4 Transceiver with Triple TIA Termination and Power-Saving Addition-Only Driving for Parallel Memory Interface Channels *Junsen He, Kiho Seong, Donghyun Yoon, Seung-Myeong Yu, Junyoung Song, Youngdon Choi, Youngdon Choi, Tony Tae-Hyoung Kim*
2671	1.4	A 0.69-pJ/Bit 16/24/32-Gb/s/pin NRZ/PAM-3/PAM-4 Multi-Mode Transmitter with Power-Optimal Rx Termination and Clock-Embedded DBI *Chengrui Gu, Dingguo Zhang, Chao Yang, Jing Jin, Howard C. Yang, Jianjun Zhou*
2713	15.11	A Resource-Efficient and Low- Latency Multi- Tap DFE with Soft- Decision for PAM4 Receiver *Junyu Lin, Jian Yu, Ning Chen, Tianqin Ye, Lei Shen*

Hardware Security for Internet-of-Things, Cyber-Physical Systems I Session

Session Code:	**A2L-04**	**Date & Time:**	**Monday May 25, 2026 (10:30 - 12:00)**
Location:	**3D**	**Chairs:**	**Preet Yadav, Yeong-Kang Lai**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1651	2.6	A Phase Delay Comparison-Based TRNG Controlled by TDC *Liang Yao, Peiyang Kang, Jin Yan, Ying Zhang, Yingchun Lu, Huaguo Liang*
1733	2.6	InFuzz: An Efficient and Lightweight In-Memory-Computing Cryptographic Fuzzy Extractor for IoT Security *Jing Kou, He Jiang, Liang Zhang, Boyi Zhang, Yang Sun, Hua Guo, Wang Kang*
2003	2.6	Planting CRYSTALS-Kyber Acceleration Seeds *Ryan Bevin, Ayesha Khalid, Seog Chung Seo, Maire O'Neill*
2667	2.6	RRAM Based CIM, PUF and True Random Number Generator for High-Security AES Encryption System *Kefan Tao, Shiyue Song, Yading Yi, Ao Shi, Haokai Guan, Lianliang Wu, Hao Ai, Lifeng Liu, Yulin Feng, Peng Huang*
2749	2.6	An ASIC Implementation of a Generalized Galois RO-PUF for Edge Device Identification *Raúl Aparicio-Téllez, Abel Naya-Forcano, Miguel Garcia-Bosque, Santiago Celma*



SoC, NoC, Multi-Core, and 3D/2.5D Integrated Circuits and Systems I Session

Session Code:	**A2L-05**	**Date & Time:**	**Monday May 25, 2026 (10:30 - 12:00)**
Location:	**3E**	**Chairs:**	**Fakhrul Zaman Rokhani, Danella Zhao**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1047	2.4	CoMe3D: Co-Optimizing Cache-Memory Coupling and Traffic Scheduling for Monolithic 3D Heterogeneous Systems *Jingpeng Ma, Ke Han, Mingxuan Wu, Rongrong Fu, Min Luo, Kuihan Zhou*
1233	2.4	Communication-Aware Routerless NoC Design with Integer Linear Programming Approach *Shuang Liu, Martin Radetzki*
1678	2.4	A Lightweight Die-to-Die Interconnect with Co-Scheduling Framework for Scalable Multi-Chip Inference Accelerators *Jie Ren, Jingyang Chen, De Ma, Xiaopeng Yu, Xiaolei Zhu*
1680	2.4	Adaptive All-Digital Clock Data Calibration Circuit for Chiplet Interfaces *Zhenming Li, Pengkang Luo, Guowei Xing, Xiaowen Jiang, Wei Xi, Kai Huang*
1912	2.4	C²NoC: A Communication–Computation Coupled NoC-Based Neural Network Accelerator *Cuiyu Qi, Yi Liu, Hui Chen, Lixia Han, Chenkai Cao, Boxiang Zhang, Weiqiang Liu*

Post-Quantum Cryptography and High-Speed Links Session

Session Code:	**A2L-06**	**Date & Time:**	**Monday May 25, 2026 (10:30 - 12:00)**
Location:	**3B**	**Chairs:**	**Dur-e-Shahwar Kundi, Youngjoo Lee**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1363	3.8	OptHQC: Optimize HQC for High-Performance Post-Quantum Cryptography *Ben Dong, Hui Feng, Qian Wang*
2136	15.3	An Efficient Fully-Pipelined Hardware Architecture for Optimized Sparse Polynomial Multiplication in CRYSTALS-Dilithium *Zhengwei Wang, Bei Wang, Zeren Zhu, Chenghua Wang, Yijun Cui, Weiqiang Liu*
1270	3.8	Deep Learning-Based Public Template Attack Against ML-DSA on ARM Microcontrollers *Yuhan Zhao, Zehua Qiao, Wei Cheng, Yuejun Liu, Yongbin Zhou*
2155	3.1	Phase Noise Integration Limits for Jitter Estimation in Wireline Transmitters *Kshitiz Tyagi, Behzad Razavi*
2933	3.1	A 50/25/12.5 Gb/s Fast-Settling Burst-Mode Transimpedance Amplifier for 50G-PON *Wenxin Zhang, Zhixin Zhang, Yifei Xia, Ruixuan Yang, Li Geng, Dan Li*

Integrated Power Circuits and Charge Pumps Session

Session Code:	**A2L-07**	**Date & Time:**	**Monday May 25, 2026 (10:30 - 12:00)**
Location:	**3G**	**Chairs:**	**Xiaolu Lucia Li, Yang Jiang**

Papers are listed in the order they will be presented.

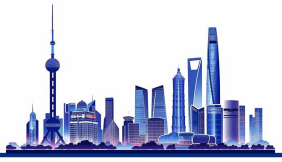
Paper Id	Topic	Title/Author
1021	4.1	A 50-ns Response Time High-Side Current Sense with a Novel Analog Level-Shifting Technique for a 100-V Monolithic 1-μm GaN-on-Si Half Bridge *Tommaso Francesco Tardani, Andrea Gambero, Sandro Rossi, Antonio Aprile, Elisabetta Moisello, Giulio Ricotti, Edoardo Bonizzoni, Piero Malcovati*
2040	4.1	A Fully-Integrated Flip-Voltage-Follower LDO with Bootstrap Follower Achieving -52 dB PSRR@1MHz and 3.24 ps FoM *Yichen Liu, Keqing Qiu, Jian Zhang, Chuang Wang, Yan Wang*
1667	4.1	A Direct 48-1 V Three-Phase Three-Inductor Converter with 5× Ton Extension and 4× V·A Metric Reduction *Zuyue Pang, Shaowei Zhen, Guanzhi Chen, Chi Zhang, Shuhai Chen, Chenguang Lv, Xiaochuan Deng, Bo Zhang*
2231	4.1	A Dual-Hysteresis Synthetic Current Control in a Single-Inductor Multiple-Output Converter for Dynamic Voltage Scaling and 0.02mV/mA Cross Regulation *Meng-Zhen Liu, Chieh-Sheng Hung, Yu-Tse Shih, Xiao-Quan Wu, Ya-Ting Hsu, Ke-Horng Chen, Ying-Hsi Lin, Shian-Ru Lin, Tsung-Yen Tsai, Xi Zhu*
2234	4.1	A Dynamic Buffer Region for 0.104 to 9.6 Wide Voltage Conversion Range in an Extensive Current Optimization Buck-Boost Converter for USB PD 3.2 *Yen-An Tsai, Yu-Teng Liang, Ya-Ting Hsu, Ke-Horng Chen, Xi Zhu, Ying-Hsi Lin, Shian-Ru Lin, Tsung-Yen Tsai*

Ferroelectric and Memristive in-Memory Computing Session

Session Code:	**A2L-08**	**Date & Time:**	**Monday May 25, 2026 (10:30 - 12:00)**
Location:	**5C**	**Chairs:**	**Kyeong-Sik Min, Vasilis Ntinas**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2689	5.6	RRAM-Based CAM for Energy-Efficient In-Memory Text Compression System *Lianliang Wu, Hao Ai, Yiyang Chen, Ao Shi, Siyuan Chen, Haokai Guan, Nan Tang, Yi Xiao, Kexun Li, Kefan Tao, Yulin Feng, Zongwei Wang, Yimao Cai, Peng Huang*
2017	5.6	A Scaling Annealing Method for Combinatorial Optimization in Asynchronous Memristive Hopfield Network *Han Bao, Kehong Xu, Yibai Xue, Zhiwei Zhou, Yuyang Fu, Jiancong Li, Jia Chen, Yi Li, Xiangshui Miao*
1090	5.6	Phase-Change Memory Based Passive Timing Circuits for DRAM Refresh Management *Anjunyi Fan, Yingming Lu, Guangyu Sun, Bing Li, Bonan Yan, Yuchao Yang*
1273	5.9	Electronic-Photonic Hybrid CIM-Based Ising Machine with Interaction-Aware Update Strategy for Combinatorial Optimization Problems *Ruihao He, Cong Wang, Liangcheng Zhao, Zefeng Xu, Hongwu Jiang*
2759	5.9	ADC-Based Nonlinear Quantization for In-Memory Computing Using FeFETs *Nellie Laleni, Thomas Kämpfe, Taekwang Jang*



Spiking Neural Network Architectures and Learning Session

Session Code:	**A2L-09**	**Date & Time:**	**Monday May 25, 2026 (10:30 - 12:00)**
Location:	**5F**	**Chair:**	**Qinyu Chen**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1085	8.2	SNNQ: Post-Training Quantization Towards Ultra Low-Bit and Fast Spiking Neural Networks *Wenlun Zhang, Kentaro Yoshioka*
1322	8.3	Training Slow Silicon Neurons to Control Extremely Fast Robots with Spiking Reinforcement Learning *Irene Ambrosini, Ingo Blakowski, Dmitrii Zendrikov, Cristiano Capone, Luna Gava, Giacomo Indiveri, Chiara De Luca, Chiara Bartolozzi*
1497	8.3	An Efficient Training Method for Memristor-Based Emergent Attractor Network *Yongxiang Li, Shiqing Wang, Zhong Sun*
1931	8.2	Power-Efficient Spiking Conversion of Deep Unfolded Transformers *Ahmed Sadaqa, Brent De Weerdt, Ruiqi Chen, Nikos Deligiannis, Bruno Da Silva*
2920	8.2	Mutual Information Loss for Enhancing Class-Wise Representation in Spiking Neural Networks *Yiling Yang, Yirong Kan, Renyuan Zhang, Yasuhiko Nakashima*

Image and Vision Sensors I Session

Session Code:	**A2L-10**	**Date & Time:**	**Monday May 25, 2026 (10:30 - 12:00)**
Location:	**5D**	**Chairs:**	**Ricardo Carmona Galan, Joseph Schmitz**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1210	7.4	VIR-EH: An Ultra-Low-Power Wide-Spectrum Visible-Infrared Vision Processing Chip with On-Chip Energy Harvesting *Zhilin Tan, Hengrui Guo, Weihao Shan, Liang Chen, Qi Wei, Jinshui Miao, Fei Qiao*
2174	7.10	A Power-Efficient 5x Compressive Sensing Readout IC for 3D-Stacked CMOS Image Sensor *Jiajia Cui, Kwok Cheong Li, Zhiyuan Wu, Yandong He, Linxiao Shen*
1186	7.3	A 0.67 e- rms Temporal-Readout-Noise 80 dB Intra-Scene High Dynamic Range CMOS Image Sensor *Pengfei Xu, Idham Hafizh, Guy Meynants*
1483	7.3	Background Calibration of Spatial Black-Level Nonuniformity for Automotive Image Sensors *Haneol Seo, Kyung-Min Kim, Min-Sun Keel, Juhyun Ko*
1754	7.7	Robust Compression Circuit for Real-Time Read-Out of 320x240 SPAD Array Based on FPGA *Yaoqi Bao, Yitian Zhang, Zhuang Yan, Dong Li, Lichen Feng, Rui Ma, Zhangming Zhu*

Acellerators for Machine Learning Session

Session Code:	**A2L-11**	**Date & Time:**	**Monday May 25, 2026 (10:30 - 12:00)**
Location:	**5H**	**Chair:**	**Walter Leon Salas**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1841	14.2	FlexCNN: Design of a Universal and Easy-to-Deploy CNN Acceleration System *Zhenjiao Chen, Jianbo Gao, Jinhao Liu, Yuhan Zhang, Ying Wang, Binghe Ma, Xudong Huang*
2769	14.2	SeVeDo: A Heterogeneous Transformer Accelerator for Low-Bit Inference via Hierarchical Group Quantization and SVD-Guided Mixed Precision *Yuseon Choi, Sangjin Kim, Jungjun Oh, Byeongcheol Kim, Hoi-Jun Yoo*
1450	14.2	A 16 nm 1.60TOPS/W High Utilization DNN Accelerator with 3D Spatial Data Reuse and Efficient Shared Memory Access *Xiaoling Yi, Ryan Antonio, Yunhao Deng, Fanchen Kong, Joren Dumoulin, Jun Yin, Marian Verhelst*
1553	14.2	NMSAcc: An Arch-Decoupled Non-Maximum Suppression Accelerator on Edge Devices *Xu Liu, Zheng Wang, Qiawei Zheng, Jinghan Zhou, Chao Chen*
1440	14.2	FPGA-Accelerated Fully Spectral CNNs for Real-Time Semantic Segmentation *Shuanglong Liu, Yaan Zhou, Haoxuan Yuan, Runjie He, Junye Jiang*

Representation and Compression for Vision and Multimodal Learning Systems Session

Session Code:	**A2L-12**	**Date & Time:**	**Monday May 25, 2026 (10:30 - 12:00)**
Location:	**5E**	**Chair:**	**Shiqi Wang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1460	12.11	Indoor Panoramic Depth Estimation via Dual-Projection Feature Fusion and Structural Refinement *Bowen Sun, Peng Li, Anthony Trioux, Zhe Li, Yun Liang, Jinyu Wang*
1560	12.11	DiffPCGC: Efficient Point Cloud Geometry Compression via Diffusion Models *Huiming Zheng, Wei Gao*
1876	12.9	Source Free Domain Adaptation for 3D Cross-Modal Semantic Segmentation *Zhuo Chen, Jianshe Duan, Yachao Zhang, Yuehui Qu, Xiaopei Zhang, Yanyun Qu*
2768	12.11	Adaptive AV2 In-Loop Filtering via Guided Neural Model with Vectorized Quantization *Kequan Mao, Dandan Ding, Urvang Joshi, Debargha Mukherjee*
2979	12.11	Efficient Token Compression for the Understanding and Generation Unified MLLMs *Junyan Lin, Jinming Liu, Shengyang Zhao, Xin Jin*

Synergies between Emerging AI Technologies and Circuits and Systems Session

Session Code:	**A2L-13**	**Date & Time:**	**Monday May 25, 2026 (10:30 - 12:00)**
Location:	**5A**	**Chairs:**	**Adam Liu, Yue Zhang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1592	15.14	Breaking the Local Optima Barrier in Branch Predictor Design Space Exploration: An LLM-Based Initialization Strategy for PSO *Qingchen Zhai, Chen Xu, Yuanyang Xiang, Weiying Wang, Yueyue Wang, Kunyu Zong, Jingshuai Jiang, Ruozhou Xiao, Zhiwei Zhang*
1415	15.14	Reinforcement-Learning-Based Multiport Circuit Topology Derivation with No Cross Regulation *Zhigao Liang, Xiaolu Li*
2644	15.14	Impact of AI Data Center Load Dynamics on Blackout Risk *Dong Liu, Biwei Li, Jingxi Yang, Tianhao Qie*
2743	15.14	Transient Stability Prediction for AC Microgrids Using a Data-Driven Approach *Zhenxi Wu, Hua Han, Jingxi Yang, Dong Liu, Biwei Li*
1404	15.14	An Agent Framework for Fault Recovery Planning Generation Based on Model Context Protocol *Tiechui Yao, He Yang, Zihao Wan, Jiannan Xu, Yishen Wang, Xi Chen, Baohua Zhao*

AI for Medical Signal and Image Analysis Session

Session Code:	**A2L-14**	**Date & Time:**	**Monday May 25, 2026 (10:30 - 12:00)**
Location:	**5B**	**Chairs:**	**Mohamad Sawan, Yunshan Zhang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1303	6.8	Slice-Aware Sampling in CS-Based Deep Learning Brain MRI Reconstruction *Elisabetta Spinazzola, Luciano Prono, Fabio Pareschi, Riccardo Rovatti, Gianluca Setti*
2083	6.8	Video-Based Gait Analysis for Lumbar Disc Herniation Screening *Sixu Tao, Jin Ai, Menghan Hu, Jian Zhang*
2245	6.7	Respiratory Disease Prediction from Lung Sounds Using Reservoir Computing *Tushar Gupta, Vasundhara Damodaran, Jose Sanchez, Arindam Sanyal*
2850	6.6	Rethinking ETI Sensing: Analysis, Experimental Proof, and Circuit Insights for In-Band, Magnitude-Only Motion Tracking in EEG *Samira Nabavi, Hossein Kassiri*

AI-Assisted and Emerging Analog Circuits Session

Session Code:	**A4L-01**	**Date & Time:**	**Monday May 25, 2026 (15:00 - 16:30)**
Location:	**3C**	**Chairs:**	**Gordon Roberts, Liangjian Lyu**

Papers are listed in the order they will be presented.

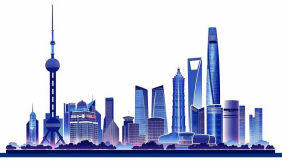
Paper Id	Topic	Title/Author
2909	1.1	A 51-nW Feature Extraction Analog Front-End for Voice Activity Detection *Xuhaohan Wang, Zirui Dong, Xing Wu, Liangjian Lyu*
1977	1.8	DDTST-Encoder: A Novel Dual-Domain Time-Series Transformer Encoder for Analog Circuit Fault Diagnosis *Naixin Zhou, Yijiu Zhao, Shibo Chen*
2086	1.8	Ising-ReRAM: A Low Power Ising Machine ReRAM Crossbar for NP Problems *Everest Bloomer, Irem Didin, Ching-Yi Lin, Sahil Shah*
2092	1.8	Automatic Circuit Topology Generation on a Reconfigurable Analog Array *Ziyi Chen, Ioannis Savidis*
2060	1.2	An Inductorless Downconversion Mixer with 24.2-dB CG, 8.2-dB NF, 350-μW Power, and 50-Hz Flicker-Noise Corner Frequency at −5-dBm LO *Saeed Ghaneei Aarani, Amin Beigi, Frederic Nabki, Shahriar Mirabbasi, Benoit Gosselin*

Pipeline and Non-Conventional ADC Architectures Session

Session Code:	**A4L-02**	**Date & Time:**	**Monday May 25, 2026 (15:00 - 16:30)**
Location:	**3I+3J**	**Chairs:**	**Jorge Fernandes, Edoardo Bonizzoni**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1256	1.3	A Reconfigurable VCO-Ringamp Based Pipeline ADC *Amartya Basak, Runpeng Gao, Ahmed AbdelRahman, Aniruddha Sriram, Un-Ku Moon*
1280	1.3	A KT/C-Noise-Cancelled Charge-Sharing Sampling Pipeline ADC Front-End with Parallel Operation Timing and Substrate-Tracking Technique *Shiang Li, Wen Jia, Jingpeng Zhou, Peng Wang, Fule Li, Zhihua Wang*
2940	1.3	A Single Channel Two-Stage 12b 500MS/s Pipelined-SAR ADC with Reset-Independent Asynchronous SAR Logic and Differential Flipped Voltage Follower Based Two-Stage Open-Loop Dynamic Amplifier *Qing Su, Wenhao Ren, Jingyuan Xu, Xuan Guo, Hanbo Jia, Xuqiang Zheng, Linzhen Wu, Kai Sun, Nan Sun, Xinyu Liu*
1500	1.3	An 11.5-Bit ENOB 312.5kS/s Column-Parallel Two-Step Single-Slope ADC for Infrared Focal Plane Readout Circuit *Zijian Wang, Yao Li, Qiuwei Wang, Yiqiang Zhao*
2129	1.3	A Low-Power, Single-Comparator, Differential Level-Crossing ADC *Farnaz Salarkia, Tor Sverre Lande, Snorre Aunet, Dag Trygve Eckhoff Wisland*



Voltage References and Power Management Session

Session Code:	**A4L-03**	**Date & Time:**	**Monday May 25, 2026 (15:00 - 16:30)**
Location:	**3A**	**Chairs:**	**Filippo Neri, Bibhu Sahoo**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1891	1.5	A 0.07-mm2 32.7-kHz Frequency Reference with Aging Calibration Embedded 1-Second Timer Scoring 22% Residual Error After 500-Hour Aging at 150°C in 28-nm CMOS *Zhicheng Dong, Huajin Sun, Xiaoteng Zhao, Yuxing Qi, Zekai Yang, Xianting Su, Rong Zhou, Bowen Wang, Ruixue Ding, Shubin Liu, Zhangming Zhu*
2782	1.5	A Pico-Watt, Supply-Insensitive All CMOS Voltage Reference, from -30◦C to 160◦C for Ultra Low Power IoT Applications *Soham Bhattacharyya, Anubhab Banerjee, Zia Abbas*
2949	1.5	A 40 µV VRipple, 0.1-ps FoM Output-Capacitor-Less Fully Time-Domain Digital LDO with a VCO-Assisted Dual Loop *Guanzhe Hu, Shengping Lv, Yufei Song, Peng Zhang, Wen Jia, Fei Chen, Shuqiang Lu, Zhihua Wang, Hanjun Jiang*
2690	1.5	PVT Robust LDO with Curvature Compensated BGR Over Wide Temperature Range -55°C to 170°C *Juturu Dhanush, Zia Abbas*
1079	1.8	A Fast TX/RX Switching Power Management Unit with Capless Sink/Source LDO for Heterogeneous mmWave Phased Arrays *Yuchen Ai, Xuyang Lu*

Datapath & Arithmetic Circuits and Systems I Session

Session Code:	**A4L-04**	**Date & Time:**	**Monday May 25, 2026 (15:00 - 16:30)**
Location:	**3D**	**Chairs:**	**Ettore Napoli, Hao Zhang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1119	2.1	High-Speed Area-Efficient Adder Design with SET-MOS Technology *Jingping Zhang, Chunhong Chen*
1296	2.1	First Demonstration of Ternary Logic Circuits in Commercial 180-nm CMOS Technology *Guangchao Zhao, Keyi Liao, Zijian Wang, Zihai Zhan, Xingyu Huang, Xingli Wang, Beng Kang Tay, Mingqiang Huang*
1457	2.1	High-Throughput and Configurable Modular Multiplier Using Extended Montgomery Reduction *Yueqin Dai, Minghao Li, Zhongfeng Wang, Xiaodong Yan, Jie Song*
1612	2.1	A High-Performance and Area-Efficient Unified Butterfly Module for ML-KEM Polynomial Computations *Chun-Jui Kang, Wai-Chi Fang*
1721	2.1	UniMAC: Multi-Precision MAC with a Unified Computing Architecture for Efficient Large Language Model Inference *Xiao Cong, Xingyuan Hu, Juntao Liu, Xulong Zhang, Haoran Geng, Qi Wu, Yuan Du, Li Du*

SoC, NoC, Multi-Core, and 3D/2.5D Integrated Circuits and Systems II Session

Session Code:	**A4L-05**	**Date & Time:**	**Monday May 25, 2026 (15:00 - 16:30)**
Location:	**3E**	**Chairs:**	**Huiyun Li, Fakhrul Zaman Rokhani**

Papers are listed in the order they will be presented.

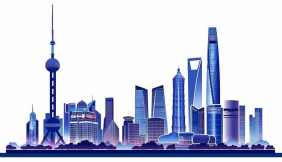
Paper Id	Topic	Title/Author
2070	2.4	Low-Loss CNN Acceleration Scheme Based on Optical Network-on-Chip (ONoC) *Wen Yang, Chunfang Tu, Yang Li*
2077	2.4	CHiP-NoC: A Congestion-Adaptive Dual-Mode Neuromorphic NoC with Hybrid Spike Compression *Yipeng Gao, Yi Zhong, Yingying Cui, Song Jia, Yuan Wang*
2114	2.4	High-Speed Bufferless NoC-Based LLM Accelerator with Distributed Ring-Shaped Buffer *Kun-Chih Chen, Bo-Chun Chen*
2321	2.4	LIRL-NoC: Long-Range Link Insertion Using Reinforcement Learning for Network-on-Chips *Yiqun Lang, Tiejun Li, Yuhan Tang, Lizhou Wu, Sheng Ma, Jianmin Zhang, Yunping Zhao*
2809	2.4	A Fully Digital and Bias-Free Ternary Bus for Energy-Efficient On-Chip Interconnects *Yesong Jeong, Myoung Kim, Woo-Seok Kim, Junyoung Park, Min Woo Ryu, Kyung Rok Kim*

Wireless Communications I Session

Session Code:	**A4L-06**	**Date & Time:**	**Monday May 25, 2026 (15:00 - 16:30)**
Location:	**3B**	**Chairs:**	**Jienan Chen, Shan Cao**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1799	3.2	Low-Latency Software-Defined 5G NR PUSCH Receiver with Mixed-Precision SIMD Acceleration *Jaehee Kim, Chanhee Lee, Jaewha Kim, Nam-Il Kim, Youngjoo Lee*
1356	3.5	Detector-in-Memory for Massive MIMO Detection *Ryan Fu, Mihir Kavishwar, Naresh Shanbhag*
2103	3.7	Memory-Efficient Partially Self-Corrected Min-Sum LDPC Decoder for 5G NR Applications *Seungjun Kim, Sangbu Yun, Jeongwon Choe, Youngjoo Lee*
1083	3.2	Low-Complexity and Resource-Efficient Design of a Streaming Channel Estimation for ZP-OTFS *Simone Acciarito, Gian Carlo Cardarilli, Luca Di Nunzio, Riccardo La Cesa, Marco Re, Sergio Spanò, Cristian Valenti*
1158	15.5	Spatio-Temporal Event Clustering for Tracking Moving Light Sources in Event-Camera Visible Light Communication *Zhengqiang Tang, Tadahiro Wada, Shintaro Arai, Shan Lu, Takaya Yamazato*



High Efficiency Converters and Drive Circuits for Specialized Applications Session

Session Code:	**A4L-07**	**Date & Time:**	**Monday May 25, 2026 (15:00 - 16:30)**
Location:	**3G**	**Chair:**	**Mo Huang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1601	4.1	An Ultra-Low Quiescent Current Step-Down DC-DC Converter for Heavy Load Automotive Applications *Bohang Zheng, Liang Zhou, Tianjiao Zhang, Ho Chung Yan, Yong Zhou*
1011	4.4	An All-NMOS Adaptive Active Gate Driver with Detection-Free CSIV Spike Suppression *L S S Pavan Chodisetti, Wei-En Chiu, Ming-Chi Chou, Chua-Chin Wang*
1550	4.4	A Multi-Stage SiC Gate Driver Utilizing Peak/Valley Miller Plateau Voltage Tracking for 48.4% Switching Loss Reduction *Weijia Hao, Run Min, Desheng Zhang, Jianming Lei, Han Peng, Qiaoling Tong*
2436	4.4	A 267-mV Input and 122-ns Fall Time, Pre-Charged Cross-Coupled Pulse Voltage Doubler for Low-Voltage Thermoelectric Energy Harvesting *Jingbo Li, Naoki Kurisu, Daisuke Kanemoto, Tetsuya Hirose*
2653	4.4	A Fully Integrated Gate Driver with Closed-Loop Feedback Achieving Wide Output Range Using Low-VGS Devices *Zibin Guo, Yuzhou Mao, Zhengyu Zhu, Jiaming Li, Quan Sun, Yanzhao Ma*

Spintronics-based In-Memory Computing Session

Session Code:	**A4L-08**	**Date & Time:**	**Monday May 25, 2026 (15:00 - 16:30)**
Location:	**5C**	**Chairs:**	**Hongwu Jiang, Vasilis Ntinas**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1743	5.5	An Event-Driven Spiking Compute-in-Memory Macro Based on SOT-MRAM *Deyang Yu, Chenchen Liu, Chuanjie Zhang, Xiao Fang, Weisheng Zhao*
2735	5.5	A Fully-Parallel Digital MRAM Computing-in-Memory Macro Featuring a High-Efficient Dynamic Adder Tree and Bit-Splitting MAC *Zhongzhen Tong, Jiye Yao, Shaohui Ma, Yulong Qiu, Zhaohao Wang, Amara Amara, Xiaoyang Lin*
2793	5.5	A Low-Power CMOS–Spintronic Neuromorphic Network Based on Vortex Oscillators *Hossein Esmailbeygi, Dario Fernandez-Khatiboun, Ravish Kumar Raj, Elham Hatamzadeh, Farshad Moradi*
2901	5.5	Multi-Retention and Bit-Level Approximate STT-MRAM for High-Efficiency AI Applications *Yulong Qiu, Chao Wang, Weimeng Zhao, Zhongzhen Tong, Zhaohao Wang*
1194	5.5	SIMCH: Stochastic In-Memory Computing Using High-Density MTJ *Tianqi Zhang, Qiuyuan Wang, Flavio Ponzina, Luqiao Liu, Tajana Rosing*

Neuromorphic Circuits and Neuron Implementations Session

Session Code:	**A4L-09**	**Date & Time:**	**Monday May 25, 2026 (15:00 - 16:30)**
Location:	**5F**	**Chair:**	**Jim Harkin**

Papers are listed in the order they will be presented.

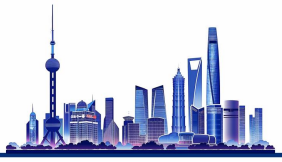
Paper Id	Topic	Title/Author
1633	8.8	An Asynchronous Mixed-Signal Resonate-and-Fire Neuron *Giuseppe Leo, Paolo Gibertini, Irem Ilter, Erika Covi, Ole Richter, Elisabetta Chicca*
2855	8.3	Configurable p-Neurons Using Modular p-Bits *Saleh Bunaiyan, Mohammad Alsharif, Abdelrahman S. Abdelrahman, Hesham ElSawy, Suraj S. Cheema, Suhaib A. Fahmy, Kerem Y. Camsari, Feras Al-Dirini*
2870	8.3	Adiabatic Energy-Recycling Charge-Redistribution Array for Ultra-Low Power Massively Parallel Cross-Correlation *Shashank Bansal, Pal Gunnar Hogganvik, Soumil Jain, Gopabandu Hota, Bouchaib Cherif, Johannes Leugering, Gert Cauwenberghs*
2988	8.8	A Linear Analog Resonate-and-Fire Neuron *Angqi Liu, Filippo Moro, Sebastian Billaudelle, Melika Payvand*
1949	8.8	Design-Driven Exploration of Mom Capacitors for Capacitive Neural Networks *Sachin Maheshwari, Himadri Singh Raghav, Mike Smart, Themis Prodromakis, Alexander Serb*

Biochemical and Environmental Sensors Session

Session Code:	**A4L-10**	**Date & Time:**	**Monday May 25, 2026 (15:00 - 16:30)**
Location:	**5D**	**Chairs:**	**Paula Lopez Martinez, Juan Antonio Leñero-Bardallo**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1362	7.12	Electrode-Dependent Gas Sensing Behavior of CNT-TiO_2 Hybrids for Ethanol Detection *Mostafa Shooshtari, Sten Vollebregt, Alireza Salehi, Saeideh Pahlavan, Teresa Serrano-Gotarredona, Bernabé Linares-Barranco*
1968	7.13	An Autonomous Wireless Biosensor Node for Multi-Seasonal In-Vivo Crop Monitoring *Edoardo Graiani, Michele Caselli, Valentina Bianchi, Ilaria De Munari, Andrea Boni*
2619	7.16	A Multi-Channel Readout IC with Extended Dynamic Range ADC for Fast and Portable Ion Mobility Spectrometry *Juan Campoverde, Mario Amo-González, Daoíz Zamora, Lluís Terés, Francisco Serra-Graells*
2388	7.15	A High Dynamic Range and Energy-Efficient Readout Circuit for Versatile Electrochemical Sensing *Minghui Cui, Yuntao Han, Xiongfei Jiang, Themis Prodromakis, Shiwei Wang*
2452	7.13	Design and Validation of a Wireless System for Bokashi Compost Monitoring *Luis Ruiz Gonzalez, Walter Leon-Salas, Nicolas Rendon Arias, Lori Hoagland, Mauricio Postigo-Malaga, Dennis Macedo*



Circuits, Systems and Architectures for Machine Learning I Session

Session Code:	**A4L-11**	**Date & Time:**	**Monday May 25, 2026 (15:00 - 16:30)**
Location:	**5H**	**Chair:**	**Ibrahim Elfadel**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2140	14.2	Harnessing Spatiotemporal Redundancy for Fast Diffusion Models on FPGA *Dongge Qin, Junhong Qian, Shaoqiang Lu, Yangbo Wei, Ruizhe Deng, Xiao Shi, Chen Wu, Longxing Shi, Lei He*
2293	14.2	Hardware-Efficient Softmax and Layer Normalization with Guaranteed Normalization for Edge Devices *Dawon Choi, Hana Kim, Ji-Hoon Kim*
1747	14.2	VCCU: A RISC-V-Based Edge Computing Processor Capable of General-Purpose Computing and Infrared Image Processing *Yushan Dai, Zhengyao Shi, Jian Mei, Angyang Li, Yongliang Huang, Lei Deng, Junyu Wang, Rui Yin*
1042	14.2	RACP: An Efficient RISC-V Domain-Specific Processor for Arbitrary-Size Kernel CNNs *Bowen Jiang, Jianyang Ding, Tianshuo Lu, Huachen Zhang, Xuzhuo Hu, Zhilei Chai*
2566	14.2	A Compilation Framework for Domain Specific Multi-Chiplet Systems with Double-Layer Genetic Algorithms *Qi Wu, Yichuan Bai, Chao Fang, Yuan Du, Li Du*

Architectures and Compression Techniques for Rendering, Perception, and Forecasting Session

Session Code:	**A4L-12**	**Date & Time:**	**Monday May 25, 2026 (15:00 - 16:30)**
Location:	**5E**	**Chairs:**	**Li Li, Xin Lou**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1991	12.2	Topic-Guided and Context-Accumulated Conditions for Prompt Compression *Yenan Xu, Changsheng Gao, Li Li, Dong Liu*
2259	12.10	ZeroBlade: A Spatial Similarity-Aware HiSparse MLP Engine for Neural Volume Rendering *Antong Li, Haochuan Wan, Xiangyu Zhang, Xin Lou*
2290	12.17	LiDAR-Based Framework for Detecting Suspicious Human Activities *Ahd Aljumah, Charalampos Antoniadis, Hakim Ghazzai, Nawfal Guefrachi, Ahmad Alsharoa, Gianluca Setti*
2350	12.14	TFAF: Temporal–Frequency Attention Fusion for Transformer Pretraining in Time Series Forecasting *Weisen Cheng, Ming Xue, Binchuan Zhang, Luyao Zhang, Pengfei Wang, Xiaofei Yang, Yudong Fang, Jing Li*
2366	12.10	SCAR: A Neural Rendering Accelerator with Sparse-Aware Sampling and Conflict-Free Encoding *Yunxiang He, Chaofan Li, Yongzhi Zhang, Qihan Ding, Quanyu Chen, Xin Lou*

Artificial Intelligence in Power and Energy Circuits and Systems I Session

Session Code:	**A4L-13**	**Date & Time:**	**Monday May 25, 2026 (15:00 - 16:30)**
Location:	**5A**	**Chair:**	**Herbert Iu**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1690	15.4	Reinforcement Learning–Based Optimal Scheduling for Virtual Power Plant Participation in Energy and Regulation Markets *Yu Chen, Miaoyuan Wang, Ying Ma, Xin Lei, Samson S Yu, Zhen Li*
1746	15.4	A Reinforcement Learning Co-Simulation Platform for Event-Triggered and Variable-Frequency Power Converter Control *Li Chen, Minggang Chen, Qinsong Qian, Weifeng Sun*
2462	15.4	Parallel Critic-Free Reinforcement Learning with Direct Parameter Space Mapping for Large-Scale Analog LDO Sizing *Han Wu, Haoning Jiang, Ziheng Wang, Zhuoli Ouyang, Chen Hu, Bo Yuan, Yan Lu, Junmin Jiang*
1873	15.4	Entity-Aware Graph Neural Network for Multi-Intent Spoken Language Understanding in Power Dispatch Systems *Lei Wang, Chao Ma, Xin Li*
2021	15.4	Condition Monitoring of IGBT in Three-Phase Inverters Based on Convolutional Neural Network Algorithm *Yang Liu, Zhaoyang Zhao, Jingqi Liu, Wenkang Zhou, Weicheng Wang, Yuting Liu, Yunfei Wang, Herbert Ho Ching Iu*

Bio-Signal Acquisition Front-Ends Session

Session Code:	**A4L-14**	**Date & Time:**	**Monday May 25, 2026 (15:00 - 16:30)**
Location:	**5B**	**Chairs:**	**Hua Fan, Jiangchao Wu**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1379	6.6	A Low-Channel-Crosstalk Orthogonal Time-Division Multiplexing AFE for Bio-Signal Acquisition *Jie Yin, Xiangyi Liu, Yinuo Zhang, Shaofei Wu, Xufeng Liao, Zhangming Zhu, Lianxi Liu*
2237	6.4	A Low-Power High-Impedance Instrumentation Amplifier with Capacitor-Calibration for Bio-Sensors *Feng Yan, Bingjun Xiong, Weijie Ge, Kangkang Sun, Jingjing Liu*
2346	6.1	A Power-and-Area Efficient AFE with Continuous Time-Gain Compensation of 48dB Gain Range and ±0.6dB Gain Error for Miniature Ultrasound Probes *Li Dai, Zhenghan Xing, Jinlai Fu, Yihu Yu, Zhong Zhang, Kejun Wu, Ning Ning, Jing Li, Qi Yu*
2722	6.1	A 4.7 μW Dual-Phase Front End with Dual-Mode Buffer for Dry-Electrode ECG Acquisition *Ao Luo, Zhechang Hu, Pujia Xing, Lei Qian, Liang Qi, Yan Liu*
1640	6.3	A Hybrid CTDT ΔΣ Direct-Digitization Analog Front-End with SAR Quantizer Reuse Zin Boosting *Fan Luo, Wenjie Wang, Zhengtao Zhu, Longbin Zhu, Zhijun Zhou, Keping Wang*

Programmable, High-Drive, and High-Voltage Amplifiers Session

Session Code:	**A5L-01**	**Date & Time:**	**Monday May 25, 2026 (16:30-18:00)**
Location:	**3C**	**Chairs:**	**Salvatore Pennisi, Gaetano Palumbo**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1562	1.1	A 55-dB Range, 0.87-dB Step Decibel-Linear Mixed Structure Programmable Gain Amplifier Based on R-2R Resistor Array for Sensor System *Xin Hu, Kejun Wu, Fan Yu, Chenhe Zhang, Yuhan Hu, Ning Ning, Jing Li, Zhong Zhang, Qi Yu*
2502	1.1	A Single-Stage Class-AB OTA with 100-dB Gain Driving 20-pF to 8-nF Capacitive Loads *Meysam Akbari, Erika Covi, Kea-Tiong Tang*
2514	1.1	A 0.036mm² Cross-Coupled Class-AB High-Voltage Amplifier with Unipolar/Bipolar Output Using 180nm BCD for Multi-Channel MEMS Drivers *Zhen Yu, Ning Ning, Junfeng Wang, Qiling Liang, Kejun Wu, Zhong Zhang, Jing Li, Qi Yu*
1472	1.1	A 196-MHz Bandwidth Transimpedance Amplifier with High Out-of-Band Rejection Employing Transmission Zeros *Hexuan Wu, Wei Li, Yunyou Pu, Xingyu Ma, Hongtao Xu*
2872	1.1	An Adaptive SMU System with Single-Shot Transient Impedance Sensing and 1 mF Capacitive Driveability *Yinxuan Peng, Zhixuan Jiang, Shuo Xing, Yanjin Lyu, Yuanqi Hu*

Delta–Sigma ADCs and DAC Techniques Session

Session Code:	**A5L-02**	**Date & Time:**	**Monday May 25, 2026 (16:30-18:00)**
Location:	**3I+3J**	**Chairs:**	**Jose de la Rosa, Qiang Li**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2530	1.3	Wideband Cartesian RF-DAC-Based Predistorter Using Nonlinear RF-DACs and IQ Expansion *Victor Åberg, Han Zhou*
2631	1.3	Residual Convolutional Neural Networks for Digital Calibration of Oversampled ADCs *Shamma Nasrin, Matt Kinsinger, Anoop Bengaluru, Jia-Ching Chuang, Sumukh Bhanushali, Arindam Sanyal*
2417	1.3	Influence of Quantizer Resolution in Gm-C Based DSM with Feedback Non-Linearity Cancellation *Bishoy M. Zaky, John G. Kauffman, Francesco Conzatti, Maurits Ortmanns*
1168	1.3	A Stimulus-Free Foreground Calibration Technique for Correction of Feedback DAC Element Mismatch in ΔΣ-A/D Converters *Alok Baluni*
2760	1.3	A 30MHz-BW Continuous-Time Delta Sigma Modulator with Reference Rotation and Time Constant Calibration in 65nm CMOS *Zhuojian Yao, Haikun Jia, Lilan Yu, Yu Fu, Junfeng Liu, Wei Deng, Baoyong Chi*

VCO Design and Oscillator Techniques Session

Session Code:	**A5L-03**	**Date & Time:**	**Monday May 25, 2026 (16:30-18:00)**
Location:	**3A**	**Chairs:**	**Jorge Fernandes, Lei Zhang**

Papers are listed in the order they will be presented.

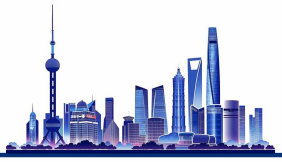
Paper Id	Topic	Title/Author
1390	1.7	A 6.12-to-8.62GHz Class-F23 VCO with Series-LC Assistance Achieving 195.9dBc/Hz FoMT at 100kHz Offset *Zihao Xia, Chenghao Liu, Zhiliang Hong, Yumei Huang*
2100	1.7	A 0.1-V Transformer-Based Class-D VCO Achieving 0.9-V Output Swing and >193.8-dBc/Hz FoM at 10-MHz Offset *Yang Li, Chuanhai Gao, Xiaoyue Cai, Xiaohua Yu, Ronghua Ni*
2125	1.7	A Series-Resonance VCO with Magnetic Mutual Impedance Achieving 191.9dBc/Hz FoM *Chengyu Yang, Jingsong Cui, Zirui Jin*
2384	1.7	An X-Band LC-VCO with 37% Tuning Range and Programmable KVCO in 65nm CMOS *Bhanu Teja Pula, Abishek Manian, Bibhu Datta Sahoo*
2896	1.7	A Quad-Core Series-Resonance VCO Enabled by Circular Lsecondary and Stacked Lprimary Achieving 198.9-dBc/Hz FoM at 10MHz *Yang Li, Dong Pu, Xiaohua Yu, Ronghua Ni*

Datapath & Arithmetic Circuits and Systems II Session

Session Code:	**A5L-04**	**Date & Time:**	**Monday May 25, 2026 (16:30-18:00)**
Location:	**3D**	**Chairs:**	**Hao Zhang, Ettore Napoli**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1791	2.1	Approximate Signed Multiplier Designs for Efficient CNN Inference *Mengshuo Zhang, Wenhui Zhang, Xiaolu Hu, Xinkuang Geng, Honglan Jiang*
1887	2.1	A Full-Custom Time-Domain Unary Sorter for Soft-Information Decoding in 65 nm CMOS *Michel Cancalon, Ludovic Damien Blanc, Christoph Thomas Müller, Yuqi Wang, Andreas Peter Burg*
1897	2.1	A High-Performance Dual-Issue RISC-V Core Addressing Data Hazard for IoT *Xinyu Zhu, Hongge Li, Yumeng Liu, Yiping Jiang, Yinjie Song*
2166	2.1	An 8T-SRAM Near-Memory Architecture for Multiplierless Approximate DCT *Xu Wang, Ke Chen, Bi Wu, Chenggang Yan, Lixia Han, Chenghua Wang, Weiqiang Liu*
2694	2.1	Low-Latency Scaling-Free Hyperbolic CORDIC Algorithm Based on Linear Rotation Angles and Leading-One Bit Detection *Yu Xie, Jie Shao, Fei Lyu, Zongguang Yu, Weiqiang Liu, Hui Chen*



Electronic Design Automation and Physical Design I Session

Session Code:	**A5L-05**	**Date & Time:**	**Monday May 25, 2026 (16:30-18:00)**
Location:	**3E**	**Chairs:**	**Xinfei Guo, Lan-Da Van**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1060	2.9	CircuitS2L: Circuit Dataset Augmentation via Generative Featuring and Supervised Labeling *Linyu Zhu, Tsun-Ming Tseng, Yushan Pan, Qing He, Xinfei Guo*
1198	2.9	Diffusion Model Based Multi-Objective Evolutionary Algorithm for High-Level Synthesis Design Space Exploration *Runxin Lin, Shanshan Wang, Chenglong Xiao*
1271	2.9	Statistical Routing Order Optimization in Global Routing *Yuanrui Qi, Jinghao Ding, Jinjia Zhou*
1345	2.9	In Simplicity There Is Strength: The Unreasonable Effectiveness of XGBoost for Generalizable SRAM Stability Prediction *Jihene Bouhlila, Mladen Berekovic*
1498	2.9	Layout-Aware Standard Cell Synthesis via Reparameterization Multi-Task Bayesian Optimization *Zhouyang Wu, Ruiyu Lyu, Keren Zhu, Zhiang Wang, Zhaori Bi, Changhao Yan, Xuan Zeng*

Wireless Communications II Session

Session Code:	**A5L-06**	**Date & Time:**	**Monday May 25, 2026 (16:30-18:00)**
Location:	**3B**	**Chairs:**	**Shan Cao, Joungsun Park**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2412	3.10	A Perturbation-Based Low-Overhead IQ Calibration Scheme for RF Receivers *M Lakshmi Deep Chowdary, Laxmeesha Somappa, Rahul Singh*
1269	3.9	A 275pJ/Bit Fully Integrated 2.4GHz DQPSK Sub-Sampling Phase-Tracking Receiver *Yongkang Wang, Jiamin Fu, Hao Hu, Chuanshi Yang, Keping Wang, Qian Zhou, Jing Xiao, Kai Tang*
2550	3.2	A 65nm 8GHz E-PPWM/FSK IR-UWB Transceiver Achieving 2.4Gb/s Data Rate and 8.6pJ/b Energy Efficiency *Nannan Shi, Bowen Wang, Minsong Zhang, Zhimeng Zhang, Rong Zhou, Zhangming Zhu*
2072	3.9	A Passive-LoRa Tag Chip Achieving 78m Battery-Free Bidirectional Communication with Standard LoRa Devices *Xin Hu, Qijing Xiao, Weixiao Wang, Guanjie Gu, Changgui Yang, Hanli Liu, Kai Huang, Bo Zhao*
1988	3.2	A 0.1-1kbps, 9.4pJ/Bit, Wake-Up Receiver with No-Standby-Clock and Level-Crossing Comparator *Rong Zhou, Jianhang Yang, Zhen Li, Yilong Dong, Xiaoteng Zhao, Bowen Wang, Zhangming Zhu*

Circuits and Systems for Wireless Power Transfer Applications Session

Session Code:	**A5L-07**	**Date & Time:**	**Monday May 25, 2026 (16:30-18:00)**
Location:	**3G**	**Chairs:**	**Zhicong Huang, Chi-Seng Lam**

Papers are listed in the order they will be presented.

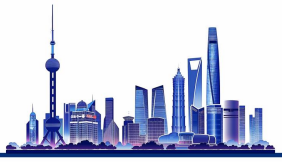
Paper Id	Topic	Title/Author
1425	4.7	A High-Efficiency Dual-Band Adaptive Power Receiver for Ultrasonic Wireless Power Transfer System Based on Dual-Frequency PMUTs *Mengyao Xu, Tongyu Zhang, Yucheng Lin, Tong Jin, Chenfang Yan, Hang Gao, Xin Liu, Zhiqiang Li*
2154	4.7	A Wireless Power and Full-Duplex Data Transfer System Achieving 57.6% End-to-End Efficiency with 0X/1X Regulating Rectifier *Sungmin Shin, Seongbin Kwon, Geonwoo Baek, Jongyeop Kim, Se-Un Shin, Franklin Bien*
2277	4.7	A Wireless Power Transfer System with Up-to-30% Efficiency Improvement Based on Fully-On/Off Global Power Control and Energy Recycling *Xunchi Liu, Yutang Chen, Yifan Lin, Yuxuan Luo, Jianping Guo*
2336	4.7	A DLSK Global Phase-Shift Controlled Wireless Power Transfer System Achieving Above 90% RX Efficiency *Fantao Wang, Wenbo Zhang, Junhong Yan, Fang An, Xiaoya Fan, Yanzhao Ma*
2542	4.7	A Dual-Output Resonant Current-Mode Wireless Power Receiver with Shared-Inductor Energy Replenishing for Neuron Stimulation *Kai Cui, Yan Lu*

Quantum Computing I Session

Session Code:	**A5L-08**	**Date & Time:**	**Monday May 25, 2026 (16:30-18:00)**
Location:	**5C**	**Chairs:**	**Georgios Ch. Sirakoulis, Vasilis Ntinas**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1003	5.7	Verification of Quantum Fourier Transform and its Inverse via Rotational and Superposition Abstraction *Arun Govindankutty, Sudarshan K. Srinivasan, Yusuf Moshood*
1174	5.7	MA-RQAOA: A System-Algorithm Co-Design Framework for Coherence-Limited Topological Quantum Computing *Xiaofei Zhao, Hua Wang*
1180	5.7	Quantum Circuit Pruning: Improving Fidelity via Compilation-Aware Circuit Approximation *Pau Escofet, Santiago Rodrigo, Rohit Sarma Sarkar, Carmen García Almudéver, Eduard Alarcón, Sergi Abadal*
2130	5.7	A Temperature-Adaptive Bias Generator with Threshold-Voltage Compensation from 3.6 K to 410 K *Yingzhe Sha, Jiaxuan Weng, Peng Wang, Zhangcheng Huang, Qi Liu*
2524	5.7	Jitter Reduction in Voltage Controlled Oscillators for Clocking at Cryogenic Temperature *Rakshith Saligram, Suman Datta, Arijit Raychowdhury*



Grand Challenge on Neural Network-based Video Coding Session

Session Code:	**A5L-09**	**Date & Time:**	**Monday May 25, 2026 (16:30-18:00)**
Location:	**5F**	**Chairs:**	**Li Zhang, Zhipin Deng**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1930	17	Efficient Video Compression with Hierarchical Motion Representation and Attentive Compensation *Shuhong Liao, Kexiang Feng, Zhimeng Huang, Siwei Ma*
2699	17	Neural-Enhanced Hybrid Video Coding: Learning-Based Motion Modeling and Adaptive In-Loop Filtering *Zhaoyu Li, Yanchen Zhao, Xu Han, Zhimeng Huang, Siwei Ma, Yun Jiang, Jiaqi Zhang*
2236	17	SRNeRV: A Scale-Wise Recursive Framework for Neural Video Representation *Jia Wang, Jun Zhu, Xinfeng Zhang*
1189	17	Neural Video Compression with Domain Transfer *Tiange Zhang, Rongqun Lin, Xiandong Meng, Haofeng Wang, Xing Tian, Qi Zhang, Siwei Ma*

Sensory Circuits and Systems I Session

Session Code:	**A5L-10**	**Date & Time:**	**Monday May 25, 2026 (16:30-18:00)**
Location:	**5D**	**Chairs:**	**Nicola Massari, Ibrahim Elfadel**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2605	7.6	Energy-Efficiency Monitoring and Parallel Fault Protection BMIC for Battery Management *Guangqian Zhu, Jiayi Yang, Wenqi Li, Wei Guo, Yongyuan Li, Yang Liu, Zhangming Zhu*
2609	7.6	A Low Power Current Sensor with 84.6dB SNR for Battery Management System *Guangqian Zhu, Shuai Hu, Xinming Huang, Wei Guo, Yongyuan Li, Yang Liu, Zhangming Zhu*
1209	7.7	Multi-Time-Gated SPAD Array with Shared TDCs for Fluorescence-Lifetime Imaging Applications *Xuanyu Qian, Chang Liu, Xianbo Li, Wei Jiang*
1492	7.1	A Differential Capacitive Sensor for Transluminal Shear Wave Elastography *Arthur Jaccottet, Antonio Gomez, Maryam Habibollahi, Andreas Demosthenous, Nader Saffari*
2859	7.9	Probabilistic Sensing: Intelligence in Data Sampling *Ibrahim Albulushi, Saleh Bunaiyan, Suraj S. Cheema, Hesham ElSawy, Feras Al-Dirini*

Circuits, Systems and Architectures for Machine Learning II Session

Session Code:	**A5L-11**	**Date & Time:**	**Monday May 25, 2026 (16:30-18:00)**
Location:	**5H**	**Chair:**	**Ricardo Carmona Galanl**

Papers are listed in the order they will be presented.

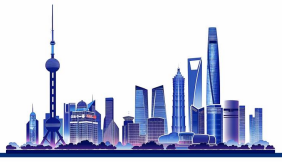
Paper Id	Topic	Title/Author
1637	14.2	A 28nm 56.45TOPS/W Hardware-Software Co-Optimized Sparse Accelerator for Traditional DNNs and Transformer-Based LLMs *Haotian Zheng, Xu Jin, Zihao Zhao, Yanhong Wang, C.-J.Richard Shi*
2789	14.2	PacViT: An Efficient ViT Accelerator with Native Dynamic Pruning and Sliding Cache Attention *Jun Gong, Zixuan Zhu, Li Tian, Yongxin Zhu*
2882	14.2	A 198.7 μj/Token Block Diffusion LLM Processor with Mask Token Similarity-Based Activation Reuse *Yujin Moon, Jiwon Choi, Seryeong Kim, Wonhoon Park, Wooyoung Jo, Yuseon Choi, Sunjoo Whang, Hoi-Jun Yoo*
2919	14.2	A 1.12 pJ/Pixel Omnidirectional Image Perception Processor Using Planar-Figure-Based Memory-Efficient Icosphere Mapping *Seungmin Lee, Donghyeon Han*
2929	14.2	A RISC-V Coprocessor to Accelerate Structured Sparse-Dense Matrix Multiplications *Rohan Krishna Vijayaraghavan, Ahmed Kamaleldin, Pruthul Pradeep Andy, Diana Göhringeri*

Multimodal Dialog, Speech Processing, and 3D Representation Session

Session Code:	**A5L-12**	**Date & Time:**	**Monday May 25, 2026 (16:30-18:00)**
Location:	**5E**	**Chair:**	**Xin Jin**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1909	12.15	A Lightweight Speaker Verification Processor Based on Large-Scale Dataset *Jui-Yang Hsu, Yun-Hwa Tsou, Tsung-Te Liu*
2512	12.11	Analysis of Converged 3D Gaussian Splatting Solutions: Density Effects and Prediction Limits *Zhendong Wang, Cihan Ruan, Jingchuan Xiao, Chuqing Shi, Wei Jiang, Wei Wang, Wenjie Liu, Nam Ling*
2670	12.5	Improved Query by Humming Using Conformer-Based Network with Harmonic-Aware Mechanism *Yu-Hsiang Kung, Kuan-Yu Chen, Jian-Jiun Ding*
2622	12.8	Stereo-NeRF: Efficient Stereo Neural Rendering via Feature Reuse *Neta Aviram, Nimrod Ginzberg, Ofer Shacham*



Artificial Intelligence in Power and Energy Circuits and Systems II Session

Session Code:	**A5L-13**	**Date & Time:**	**Monday May 25, 2026 (16:30-18:00)**
Location:	**5A**	**Chair:**	**Herbert Iu**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1494	15.4	Lightweight Quadrupolar Trapezoidal Coil Design with CNN-Accelerated Optimization for Misalignment-Tolerant IPT Converter *Zongrui Yang, Io-Wa Iam, Chi-Seng Lam*
2924	15.4	High Energy Efficiency TCAM In-Memory Search Architecture with Pre-Determined Short-Circuit Current Cutoff *Wei-Chieh Lee, Chen-Ming Lee, Chia-Wei Su, Chun-Fu Chen, I-Chieh Hsu, I-Chyn Wey, Tee Hui Teo, An-Yeu Wu*
2106	15.4	Hierarchical Super-Twisting Sliding Mode Voltage Balancing Control for IPOS-DAB Converters *Yushun Zhao, Yu Zhou, Teng Li, Luhao Song, Dongsheng Yu, Herbert Ho Ching Iu*
1992	15.4	Virtual Inertia and Damping Control Strategy for AHO Virtual Oscillator Based on RBF *Ren Yang, Zhijian Fang*
1890	15.4	Close-Loop Controlled RC Parameter Damping-Based Multiplier for Wind Farm Equivalent Modeling *Jinpeng Lei, Lingyun Yang, Zhicong Huang*

Medical Computing Hardware and SoCs Session

Session Code:	**A5L-14**	**Date & Time:**	**Monday May 25, 2026 (16:30-18:00)**
Location:	**5B**	**Chairs:**	**Jie Chen, Cheng Han**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1069	6.8	A 16-nm 24.8 Mbps/mJ Utilization-Aware Dynamic Allocation Read Mapping Accelerator for Next-Generation Sequencing *Chia-Yu Kuo, Wei-Chien Cheng, Yi-Chung Wu*
1600	6.8	A Hardware-Software Co-Design of Lightweight Polyp Segmentation Network and Ultra-Low-Power Processor for Capsule Endoscopy *Ghangmin Yun, Jaekyung Lee, Jiwon Kim, Kyungkeon Chung, Jueun Jung, Bokyoung Seo, Hyejin Lee, Junyoung Park, Kyuho Lee*
1713	6.5	A Programmable CMOS Chip for Mobile Nucleic Acid Amplification Tests *Jhan-Yi Liao, Hsi-Hao Huang, Yi-Xuan Ran, Chen-Yi Lee*
1772	6.8	A Low-Power FPGA Implementation of QRS Detection for Real-Time Heart Rate Monitoring *Weiju Wu, Chao Chen*
2583	6.8	A 0.35 mm² Fully Pipelined JPEG Encoder for Monolithic CMOS ISFET Array Integration *Lei Kuang, Junming Zeng, Pantelis Georgiou*

RF Frequency Generation and Synthesizers Session

Session Code:	**B2L-01**	**Date & Time:**	**Tuesday May 26, 2026 (10:30 - 12:00)**
Location:	**3C**	**Chairs:**	**Xi Zhu, Arindam Sanyal**

Papers are listed in the order they will be presented.

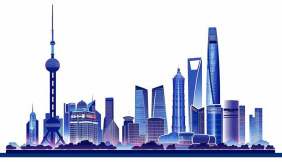
Paper Id	Topic	Title/Author
2567	1.2	Piecewise Linear Ultra-Wideband Chirp Generators for Sub-THz FMCW Radar in 28-nm CMOS *Yange Wang, Xinyu Ren, Cao Wan, Zhou Shu, Hanjun Jiang, Yuanjin Zheng*
1732	1.2	A 70 GHz Differential Noise Source for Noise Figure Built-in Self-Test in 22nm FDSOI CMOS *Fabio Pedone, Danilo Manstretta*
2283	1.2	Low-Noise Digital Fractional-N PLL with Continuous-Time Band-Pass ΔΣ TDC and Two-Point Chirp Linearization *Thi Viet Ha Nguyen, Cong Kha Pham*
2710	15.15	Cryogenic Influences on Frequency Dividers and Output Buffers in Ring-Oscillator Design and Characterization *Minda Wen, Victor Arzate Palma, Ivan O'Connell, Kevin McCarthy, Gerardo Salgado*

Time-Interleaved and High-Speed SAR ADCs Session

Session Code:	**B2L-02**	**Date & Time:**	**Tuesday May 26, 2026 (10:30 - 12:00)**
Location:	**3I+3J**	**Chairs:**	**Yi Shen, Hyeon Kim**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1435	1.3	An 8-GS/s 8-Bit 16×-Interleaved Time-Interpolator-Assisted SAR ADC in 28-nm CMOS *Dengquan Li, Yubo Yan, Zecheng Zhou, Longsheng Wang, Zhangming Zhu*
1643	1.3	A 64GS/S 8b 64× Time-Interleaved SAR ADC Achieving 33.8dB SNDR at 26GHz in 28nm CMOS *Yixiao Luo, Jiacheng Wang, Jun Chang, Hongzhi Liang, Li Dang, Ruixue Ding, Shubin Liu, Zhangming Zhu*
2316	1.3	A 1GS/s 8b 2× Time-Interleaved SAR ADC with Speed-Enhanced Techniques in 65nm CMOS *Li Dang, Yaoxin Zhang, Yuanzhe Li, Hongzhi Liang, Ruixue Ding, Shubin Liu, Zhangming Zhu*
1731	1.3	A 3.6 GS/s 7b TI-LU 2b/Cycle SAR ADC in 65 nm CMOS with Preamplifier-Level Interpolation and Shared-Reference Background Offset Calibration *Jie Zhang, Lexing Yuan, Weifeng Sun, Xueyong Zhang*
1947	1.3	A Fast Convergent Timing Mismatch Calibration for Time-Interleaved ADCs Based on Sub-Sequence Weighted Autocorrelation *Boyuan Zhang, Zhifei Lu, Xizhu Peng, Jun Zhang, Yutao Peng, He Tang, Jie Pu, Ling Qin*



Oscillators, PLLs, and Clock Generation Session

Session Code:	**B2L-03**	**Date & Time:**	**Tuesday May 26, 2026 (10:30 - 12:00)**
Location:	**3A**	**Chairs:**	**Filippo Neri, Degang Chen**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1032	1.7	A Dual-Mode Dual-Band RTWO Covering X and K Bands with Phase Interpolation Based Phase Calibration Achieving 180.4 dBc/Hz FoM *Juncheng Deng, Zhanyi Pi, Ye Wang, Yizhe Hu, Fujiang Lin, Chun-Huat Heng*
2188	1.7	A 24.3MHz RC Relaxation Oscillator with a FoM of -153.05 dBc/Hz Achieving 63ppm/°C from -40 to 125°C *Hao Hu, Yongkang Wang, Xijun Huang, Xuan Luo, Chuanshi Yang, Keping Wang, Kai Tang, Jing Xiao*
1107	1.7	A 210.6 nW FII-Based Standby Timer with Offset Compensation in 65nm CMOS for IoT Applications *Linwei Wang, Tan Peng, Kai Xu, Chaoyun Song, Rong Zhou, Zhangming Zhu*
1310	1.7	A Hyper-Extended Dual-Path Quadrature Sub-Sampling Phase Detector with Double-Cycle (720°) Phase Ambiguity Resolution *Junnan Guan, Tongde Huang, Wen Wu*
2459	15.11	A 5.7-mW 9-GHz 8-Bit Twin-PI with a Digitally-Controlled Weighted Summer in 28-nm CMOS *Changjun Zhao, Haoren Zhou, Hangyu He, Tengyang Liu, Xiaojin Li, Yang Shen, Yuhang Zhang, Yanling Shi, Bingyi Ye, Yabin Sun*

Hardware Security for Logic, Circuits and Architectures I Session

Session Code:	**B2L-04**	**Date & Time:**	**Tuesday May 26, 2026 (10:30 - 12:00)**
Location:	**3D**	**Chairs:**	**Martinez Alonso Abdel, Jing Tian**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1126	2.7	Drawbridge: Securing Early-Boot DMA Through IO Bridges *Chenyang Li, Changling Zhou, Xinhui Han*
1490	2.7	Invulnerability Checking for Memory Protection Extensions Against Meltdown *Yusuf Moshood, Sudarshan K. Srinivasan, Nimish Mathure, Arun Govindankutty*
1658	2.7	High-Performance AES-GCM Hardware via Circuit and Architecture Co-Design of AES and GHASH *Chia-Chou Chuang, Chuan-Kai Su, Ying-Sheng Huang, Da-Huei Lee, Pei-Yin Chen*
1757	2.7	Exploring Structural and Behavioral Features for Hardware Trojan Detection at Gate Level *Siyu Tian, Lingjuan Wu, Wei Hu, Hao Su, Zhongkai Huang*
1788	2.7	Precise Hardware Trojan Localization at RTL Through Graph-Based Feature Integration *Lingjuan Wu, Tianle You, Siyu Tian, Hao Su, Zhongkai Huang, Wei Hu*

Electronic Design Automation and Physical Design II Session

Session Code:	**B2L-05**	**Date & Time:**	**Tuesday May 26, 2026 (10:30 - 12:00)**
Location:	**3E**	**Chairs:**	**Bruce Sham, Kun-Chih Chen**

Papers are listed in the order they will be presented.

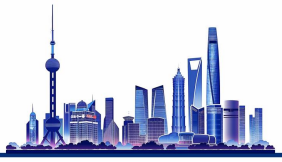
Paper Id	Topic	Title/Author
1515	2.9	Slack-Guided Arbitration for Network-on-Chip Congestion Mitigation in Boolean Processor Array Emulation *Muhan Li, Ruiyao Pu, Li Shang, Fan Yang*
1544	2.9	HGEN: A Hierarchical Layout Framework for Automated IP Integration *Heedo Jeong, Nicholas Bon, Hyungjoo Park, Andrea Bandiziol, Jaeduk Han*
1559	2.9	A Potential-Guided Efficient Timing-Driven Obstacle-Avoiding Routing Tree Algorithm *Changhao Sun, Hongxin Kong, Lang Feng*
1735	2.9	A16K: 1.6nm NSFET, FSFET, and CFET Technology Libraries for Chip-Level VLSI Prediction *Hwiryong Kim, Hanmok Park, Mingyun Sun, Yongjin Kwon, Jiyoon Jung, Gahyeon Kim, Gyeongjin Kim, Sein Kang, Sunmean Kim, Taigon Song*
1782	2.9	RC-Scaled Timing-Driven Routing: Bridging Targeted Timing Optimization and Massively Parallel Global Routing *Chuyu Wang, Zecheng Xu, Boxiang Song, Zhiang Wang, Fan Yang, Keren Zhu, Xuan Zeng*

Wireline Communications I Session

Session Code:	**B2L-06**	**Date & Time:**	**Tuesday May 26, 2026 (10:30 - 12:00)**
Location:	**3B**	**Chairs:**	**Yuan Du, Xin Peng**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2069	3.1	A 112Gb/s DAC-Based PAM-4 Transmitter with Fast Automatic Retiming Clock Phase Optimization and 6-Tap FFE in 28nm CMOS *Chenxi Han, Huajin Sun, Xiaoteng Zhao, Qi Zhang, Yuan Liu, Yuhao Zhang, Hongzhi Liang, Shubin Liu, Zhangming Zhu*
2025	3.1	A 0.57-pJ/Bit Adaptive CTLE with Novel High-Pass Node Sampling Adaptation for Wireline Receivers in 28-nm CMOS *Yudi Wang, Chang Liu, Liu Wang, Zhiwei Wei, Bo Li*
1599	3.1	Fixed-Point Implementation Analysis of MLSE Receiver DSP for High-Speed Wireline Transceivers *Dohyeon Kwon, Donggeon Kim, Yujin Choi, Yusuf Leblebici, Gain Kim*
1840	3.1	A 7×25Gb/s Transceiver Using Codebook-Based CNRZ-7 for High-Density Transmission *Ruixiao Kuai, Geng Zhang, Fangxu Lv, Jiaqing Xu, Xingyun Qi, Liangyong Yuan, Lizhou Wu, Bohui Bai, Ruotian Yin, Mingche Lai*
1224	3.1	A 26 Gb/s/pin Single-Ended Transceiver with Adaptive Switched-Capacitor-Based Simultaneous Switching Noise Compensation *Namhoon Kim, Heesang Kim, Wonbin Lee, Junghoo Kim, Sara Kim, Jaeseung Jeong, Kyeongha Kwon*



Circuits and Systems for Enhanced DC-DC Switch-mode Power Supplies Session

Session Code:	**B2L-07**	**Date & Time:**	**Tuesday May 26, 2026 (10:30 - 12:00)**
Location:	**3G**	**Chairs:**	**Yang Jiang, Yanzhao Ma**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1587	4.8	A 96.8% Peak Efficiency Dual-Path Hybrid Step-Down Converter with Full Voltage-Conversion Ratio and Reduced Inductor Current *Zibin Guo, Honglei Xu, Meng Wei, Zhitong Chen, Quan Sun, Yanzhao Ma*
2329	4.8	A Scalable Cyclically Coupled Multi-Phase Hybrid DC-DC Converter with Duty-Cycle Calibration for 48V Data-Center Power Delivery *Yuxiao Yang, Sasa Tong, Zhengxi Wang, Hanbo Tu, Zheng Yang, Ruize Sun, Zekun Zhou, Wanjun Chen, Bo Zhang*
2466	4.8	A Transient-Enhanced Buck Converter Based on Capacitor Current Adaptive On-Time (CCAOT) Control *Xiaolong Shen, Min Sun, Haolu Xie, Xing Li*
2741	4.8	An Asynchronous Ripple-Based SIMO Buck Converter with 10mV/A Cross Regulation and 1500× Unbalanced Load Current Ratio *Haoyu Hu, Guigang Cai*
2915	4.8	A Fast-Transient Buck Converter with Oversampled Multi-Phase-Ramp PWM Control *Zhenyu Shen, Xiongjie Zhang, Xiacong Liu, Yang Jiang, Rui P. Martins, Pui-In Mak*

AI Circuits and Architectures Session

Session Code:	**B2L-08**	**Date & Time:**	**Tuesday May 26, 2026 (10:30 - 12:00)**
Location:	**5C**	**Chairs:**	**Ronald Tetzlaff, Wai-Chi Fang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1179	5.1	Design Technology Co-Optimization for Digital Compute-in-Memory with Area-Efficient CFET 10T3P SRAM *Ching-Wang Yao, Fang-Yu Chang, Yu-Sheng Lai, Tao Chou, C.W. Liu*
1403	5.5	A 6.86Tb/S Bandwidth SOT-MRAM Sensing Scheme with Configurable Full-Column Over Frequency Technique for Near Memory Computing *Xinpeng Jiang, Hanting Chen, Zhaohao Wang, He Zhang, Weisheng Zhao*
2345	5.8	3D-TANoC: Thermal-Aware 3D LLM Accelerator with Hierarchical NoC and Operator-Aware Dataflow Mapping Strategy *Yuan Song, Xingyu Xu, Dengke Liu, Zihan Zou, Xilong Kang, Hui Kou, Hao Cai, Bo Liu*
2386	5.8	3D Monolithic Integrated Indium Tin Oxide-Silicon Hybrid Leaky Integrate and Fire Neuron *Harshitha Gangu, Aakash Deshpande, Ranie S. Jeyakumar, Sahil Rakesh Wani, Abhishek Ajit Kadam, Udayan Ganguly, Laxmeesha Somappa, Veeresh Deshpande*
2864	5.2	Modeling of an All-Mechanical In-Sensor Vibration Classifier Compatible with MEMS Implementation *Aleksandra Marković, Armine Karami, Hervé Fanet, Dimitri Galayko, Bernard Legrand, Philippe Basset, Gaël Pillonnet*

Compute-in-Memory-Based Neural Computing Session

Session Code:	**B2L-09**	**Date & Time:**	**Tuesday May 26, 2026 (10:30 - 12:00)**
Location:	**5F**	**Chair:**	**Di He**

Papers are listed in the order they will be presented.

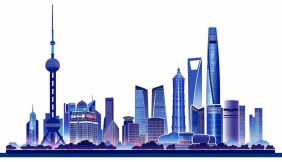
Paper Id	Topic	Title/Author
1216	8.7	Energy-Efficient Acceleration of Fourier-Based Transformers on RRAM-CIM via Mixed-Precision and DFT Symmetry *Zhiwei Zhou, Yuyang Fu, Jiancong Li, Yi Li, Xiangshui Miao*
1944	8.7	Physics-Driven In-House Memristor Crossbar Array Model for Image Classification *Daniel Veira-Canle, Masoumeh Mohammadidoghozloo, Diogo Costa, Victor Leborán, Fernando Pardo, Oscar Pereira-Rial, Francisco Rivadulla, Víctor Brea, Paula López*
2650	8.2	SRAM-Based Compute-in-Memory Accelerator for Linear-Decay Spiking Neural Networks *Hongyang Shang, Shuai Dong, Yahan Yang, Junyi Yang, Peng Zhou, Arindam Basu*
2771	8.7	High-Accuracy and Energy-Efficient RRAM-Based Real-Time Object Detection System for Thermal Infrared Imaging Applications *Kexun Li, Yiyang Chen, Ao Shi, Hairuo Lu, Lianliang Wu, Jiaqi Li, Ruiqi Chen, Yulin Feng, Lifeng Liu, Peng Huang*
2720	8.7	A Sparsity-Aware Reconfigurable Sensing-Quantization Circuit for RRAM-Based Analog Compute-in-Memory *Zhuoya Chen, Hao Ding, Yunfan Yang, Haisu Zhang, Jinshan Li, Shigeng Zhao, Yunyi Fu, Zongwei Wang, Yimao Cai*

Sensory Signal Conditioning Session

Session Code:	**B2L-10**	**Date & Time:**	**Tuesday May 26, 2026 (10:30 - 12:00)**
Location:	**5D**	**Chairs:**	**Mario Renteria Pinon, Yan Liu**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1324	7.1	An ISFET Pixel Array with Random Access Analog Floating-Gate Calibration *Roozbeh Abdollahi, Philipp Häfliger*
1642	7.16	A High-PSRR Pitch-Matched Ultrasound Receiver Analog Front-End with Integrated Beamforming for PMUT-Based Ultrasound Imaging *Tongyu Zhang, Chengrui Lv, Yazhao Mao, Yucheng Lin, Hang Gao, Xin Liu, Zhiqiang Li*
2646	7.15	A Strain-Gauge Readout Circuit with SAR-Based Current Calibration for Sensor Variation Compensation in Side-Button Applications *Dabin Yun, Sangweun Kim, Junseong Kim, Sumin Song, Minsoo Koo, Seunghoon Ko*
2825	7.2	Toward Body-Scale Tactile Sensing: A Small and Efficient Analog Front End for Matrix-Based E-Skin *Samuel Hansen, Sina Balkir, Joseph Schmitz*
1025	7.4	A 40 µW 8-Bit Accelerator Wake-Up Circuit for Always-On Smart IoT Sensor Monitoring *Andrew Ding, Sungheon Jeong, Xuyang Liu, Hamza Barkam, Shaahin Angizi, Nader Bagherzadeh, Mohsen Imani*



Quantization, Approximation, and Compression for ML Hardware I Session

Session Code:	**B2L-11**	**Date & Time:**	**Tuesday May 26, 2026 (10:30 - 12:00)**
Location:	**5H**	**Chair:**	**Milin Zhang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1423	14.2	Efficient Hardware-Oriented Approximation of Mish Activation Function and its Realization *Junting Liu, Mingyu Shu, Qiang Liu*
1476	14.1	A Multiplication-Free Floating-Point CIM Architecture with a 5-Bit Approximate Squaring Circuit *Xin Li, Juntao Ge, Miao Long, Fugui Jiang, Chenglong Duan, Yang Yang, Wenqiang Zhang, Yu Liu, Beibei Zhang, Zhiting Lin*
1655	14.1	A Floating-Point CIM Macro Featuring Asymmetric Exponent Encoding and Adaptive Mantissa Truncation for High-Efficiency AI Edge Computing *Zhiting Lin, Rongtao Li, Xiaoyu Wang, Hao Li, Xuefeng Li, Yu Liu, Xin Li, Xiulong Wu*
2091	14.1	An Approximate Digital Compute-in-Memory Macro with Reconfigurable Computational Precision for Neural Network Acceleration *Heng You, Zixiao Zhan, Yan Gao, Guanghua Zhao, Yumei Zhou, Shushan Qiao, Jia Yuan*
2202	15.7	Toward Backpropagation-Free On-Chip Training: Circuit-Algorithm Co-Design of a Goodness-Based Learning Tile *Qingchun Gong, Robert Staszewski, Bashir Al-Hashimi, Kai Xu*

Multimodal Interfaces and Efficient Architectures for Intelligent Visual Systems Session

Session Code:	**B2L-12**	**Date & Time:**	**Tuesday May 26, 2026 (10:30 - 12:00)**
Location:	**5E**	**Chair:**	**Weiyao Lin**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2311	12.11	ENnRA: A Dual-Graph Architecture with Ego-Neighbor Alignment for Multimodal Recommendation Systems *Ruixiang Yu, Zhanjie Zhang, Yicheng Di, Yuan Liu*
2331	12.10	Unity-EDR: A Hybrid Neural-Mesh Rendering System for Efficient Visual Synthesis *Zeyu Zheng, Chaolin Rao, Xiangyu Zhang, Lihua Lu, Xiaohui Zhang, Hui Wei, Xin Lou*
1366	15.5	Self-Supervised Monocular Visual Odometry Based on Multi-View Spatio-Temporal Feature Fusion *Jiaqi Liu, Zhuoling Xiao, Bo Yan*
1057	12.11	RASR: Retrieval-Augmented Super Resolution for Practical Reference-Based Image Restoration *Jiaqi Yan, Shuning Xu, Xiangyu Chen, Dell Zhang, Jiantao Zhou, Jie Tang, Gangshan Wu, Jie Liu*

Empowering the Evolving Electrical Grid: Circuits & Systems for Greener Generation, Distribution I Session

Session Code:	**B2L-13**	**Date & Time:**	**Tuesday May 26, 2026 (10:30 - 12:00)**
Location:	**5A**	**Chairs:**	**Federico Bizzarri, C. K. Michael Tse**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1278	15.9	Coupling and Clustering of Grid-Forming and Grid-Following Converters in Islanded Microgrids *Jingxi Yang, Chi K. Tse, Dong Liu*
1516	15.9	Heteroclinic Bifurcations Reveal Virtual Inertia–Damping Limits for Grid Stability *Federico Bizzarri, Angelo Maurizio Brambilla, Davide Del Giudice, Fabio Dercole, Daniele Linaro*
1939	15.9	Grid-Forming Inverters for Enhancing Grid Stability via Synthetic Inertia and Damping *Alessandro Ravera, Matteo Lodi, Alberto Oliveri, Anna Pinnarelli, Matteo Saviozzi, Marco Storace, Pasquale Vizza*
2367	15.9	A New Current Controller for Grid Following IBR Systems Using μ Transfer Functions *Álvaro Volpato, Luís Alberto*
1573	15.9	Impact of Community Structure on Robustness of Power Systems *Yuchen Wang, Wenshuang Liu, Xi Zhang, Xiwen Shan, Tiezhu Wang, Jie Yang*

Neural Recording and Stimulation ASICs Session

Session Code:	**B2L-14**	**Date & Time:**	**Tuesday May 26, 2026 (10:30 - 12:00)**
Location:	**5B**	**Chairs:**	**Sohmyung Ha, Tim Constandinou**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2081	6.4	A Reconfigurable Intracranial Multimodal Monitoring ASIC with On-Chip PVT-Insensitive Waveform Generator *Minghao Li, Zhichao Wang, Xiao Liu*
2217	6.3	A 16-Channel Rapid On-Chip Seizure Classifier with Online Re-Training for Closed-Loop Neuromodulation *Ankur Gupta, Laxmeesha Somappa*
2750	6.2	A Flexible 128-Channel Neural Stimulator with Dynamic Voltage Scaling and Synchronous Charge Balancing for Visual Cortical Prosthesis *Quynh-Trang Nguyen, Duy-Minh Nguyen, Kim-Hoang Nguyen, Xuan-Khanh Nguyen, Dang Duy Tung, Loan Pham-Nguyen, Minkyu Je*
2945	6.3	An Optimized Pre-Emphasis Spike Detector for High-Density Neural Interfaces *Jingjie Tang, Yulun Peng, Hengchang Bi, Xing Wu, C.-J.Richard Shi, Liangjian Lyu*
1046	6.8	FRRAP: A Fast-Response Reconfigurable AI Processor and its Application in Four-Class Seizure Monitoring *Heng Zhang, Qiang Tao, Chi Ben, Youbin Luo, Guoqiang He, Sirui Zhu, Jingyi Ma, Yuxiang Fu, Li Li*

RF and mm-Wave Low-Noise Amplifiers Session

Session Code:	**B4L-01**	**Date & Time:**	**Tuesday May 26, 2026 (15:00 - 16:30)**
Location:	**3C**	**Chairs:**	**Raafat Labadibi, Luis Oliveira**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1031	1.1	A Sub-6GHz Balun-LNA Using Dual Feedback gm-Boosting and Triple Path Noise Canceling Technique *Xuzhi Liu, Zhiming Chen, Zhe Xu, Lianyi Zhao, Xiaoran Li, Xinghua Wang, Zicheng Liu*
1068	1.2	A 17-39GHz Transformer-Based Noise-Cancelling LNA with 2.7-4.3dB Noise Figure in 28nm CMOS *Hao Xu, Tenghao Zou, Na Yan*
2454	1.2	A 2-18 GHz LNA Based on Dual-Mode Hybrid Coupled Frequency Response Reshaping Technique *Kuisong Wang, Henan Zhang, Yuying Zhang, Xuming Sun, Jing Wan, Shushan Qiao, Xiaoxin Liang*
2736	1.2	A 8–19-GHz Current-Reused Wideband LNA with Dual Transformer Feedback *Zushuai Xie, Haojie Gong, Guoqing Li, Tinghuan Chen, Zhikuang Cai, Zixuan Wang*
2469	1.1	A Ringamp-Based Low-Noise Bias Generation Technique *Krishnakanth R, Raymond Mabilangan, Hyungpyo Kim, Kent Edrian Lozada, Seung-Tak Ryu*

Delta–Sigma and Zoom ADCs Session

Session Code:	**B4L-02**	**Date & Time:**	**Tuesday May 26, 2026 (15:00 - 16:30)**
Location:	**3I+3J**	**Chairs:**	**Qiang Li, Jose de la Rosa**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1953	1.3	An 18-Bit 97.2-μW 40-kSPS Single-Rate Scalable Switched-Capacitor Zoom ADC with Intrinsic DAC Mismatch Immunity and Tri-Level CDAC *Yuke Shen, Bo Zhao, Jun Xiao, Deao Wu, Yuanhao Zhao, Yanbo Zhang, Yi Shen, Shubin Liu, Ruixue Ding, Zhangming Zhu*
1467	1.3	A 181.9-dB FoMSNDR Power/Bandwidth Scalable Fully Dynamic Discrete-Time Zoom ADC Using Gain Boost Floating Inverter Amplifiers *Ming Xu, Zhengyu Ren, Tianlong Gao, Chunyang Yu, Wu Gao*
1617	1.3	A Power-Efficient VCO-Based ΔΣ Modulator Achieving 175.5dB FoMs with an Active Open-Loop Integrator and Compensation-Current Linearization *Zihan Zhang, Shengdong Zhang, Zeyu Cai*
2740	1.3	A 91.4-dB SNDR 200-kSPS Exponential-Incremental ADC with an Open-Loop Ratio-Based Floating Inverter Dynamic Amplifier *Jiuhuan Feng, Yuke Shen, Bo Zhao, Yuanhao Zhao, Tao Chen, Yi Shen, Shubin Liu, Ruixue Ding, Zhangming Zhu*
1938	1.3	Bandpass Incremental Delta-Sigma ADCs *Jesko Flemming, Kaixin Tang, Bernhard Wicht, Pascal Witte*

Multiphase PLLs and Injection-Locked Clocks Session

Session Code:	**B4L-03**	**Date & Time:**	**Tuesday May 26, 2026 (15:00 - 16:30)**
Location:	**3A**	**Chairs:**	**Shahriar Mirabbasi, Robert Sobot**

Papers are listed in the order they will be presented.

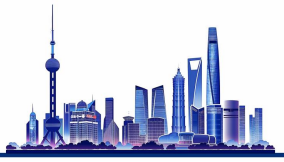
Paper Id	Topic	Title/Author
1468	1.7	A Dual-Loop Multiphase DLL with Charge-Pump-Based Duty Cycle and Phase Error Corrector *Jie Luo, Jiatong Sun, Yetong Wang, Kaixue Ma, Keping Wang*
1779	1.7	A 240-to-945MHz 8-Phase PLL Clock Synthesizer with 1.22° Skew Calibration in 180nm HV CMOS for Closed-Loop Digital SiC/GaN Gate Driving *Erik Wehr, Tobias Zekorn, Kenny Vohl, Ralf Wunderlich, Stefan Heinen*
2291	1.7	Design of Switch-Free Bias-Current-Free ΔΣ Fractional-N PLLs with Calibration-Free Quantization Noise Reduction *Howon Kim, Honggeun Park, Kang-Yoon Lee, Woogeun Rhee*
2586	1.7	An Injection-Locked Eight Phase Clock Generator with Edge Replacement and Injection Error Calibration Achieving -253.7dB FOMJitter-N *Sirou Li, Weijia Zeng, Kaiyun Cao, Liangjian Lyu, C.-J.Richard Shi, Hao Min*
1202	1.8	A 1–10.7GHz Low-Jitter 8-Phase Injection-Locked Clock Generator with Supply-Voltage Feedback in 28nm CMOS *Yu Fu, Haikun Jia, Wei Deng, Junfeng Liu, Zhuojian Yao, Angxiao Yan, Baoyong Chi*

Hardware Security for Logic, Circuits and Architectures II Session

Session Code:	**B4L-04**	**Date & Time:**	**Tuesday May 26, 2026 (15:00 - 16:30)**
Location:	**3D**	**Chairs:**	**Martinez Alonso Abdel, Xiaojin Zhao**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1845	2.7	On Evaluating the Security of Complete Access Protocol of IJTAG Architecture *Gaurav Kumar, Pardeep Kumar, Anuj Kumar, Raj Kumar Choudhary, Satyadev Ahlawat*
1957	2.7	CVA6-CFI: A First Glance at RISC-V Control-Flow Integrity Extensions *Simone Manoni, Emanuele Parisi, Riccardo Tedeschi, Davide Rossi, Andrea Acquaviva, Andrea Bartolini*
2007	2.7	DNA-HHE: Dual-Mode Near-Network Accelerator for Hybrid Homomorphic Encryption on the Edge *Yifan Zhao, Xinglong Yu, Yi Sun, Honglin Kuang, Jun Han*
2050	2.7	A Metastability-Based Reconfigurable TRNG Featuring Online Test and Auto-Calibration *Chongyao Xu, Jiale Li, Zhangming Zhu*
2172	2.7	S²2PUF: A <1.77E−8 BER Schmitt Effect SRAM PUF with Load Tilt Masking for Resource-Constrained Systems *Xijun Huang, Li Ni, Jinwei Pu, You Meng, Kai Tang*



Electronic Design Automation and Physical Design II Session

Session Code:	**B4L-05**	**Date & Time:**	**Tuesday May 26, 2026 (15:00 - 16:30)**
Location:	**3E**	**Chairs:**	**Bruce Sham, Kun-Chih Chen**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1515	2.9	Slack-Guided Arbitration for Network-on-Chip Congestion Mitigation in Boolean Processor Array Emulation *Muhan Li, Ruiyao Pu, Li Shang, Fan Yang*
1544	2.9	HGEN: A Hierarchical Layout Framework for Automated IP Integration *Heedo Jeong, Nicholas Bon, Hyungjoo Park, Andrea Bandiziol, Jaeduk Han*
1559	2.9	A Potential-Guided Efficient Timing-Driven Obstacle-Avoiding Routing Tree Algorithm *Changhao Sun, Hongxin Kong, Lang Feng*
1735	2.9	A16K: 1.6nm NSFET, FSFET, and CFET Technology Libraries for Chip-Level VLSI Prediction *Hwiryong Kim, Hanmok Park, Mingyun Sun, Yongjin Kwon, Jiyoon Jung, Gahyeon Kim, Gyeongjin Kim, Sein Kang, Sunmean Kim, Taigon Song*
1782	2.9	RC-Scaled Timing-Driven Routing: Bridging Targeted Timing Optimization and Massively Parallel Global Routing *Chuyu Wang, Zecheng Xu, Boxiang Song, Zhiang Wang, Fan Yang, Keren Zhu, Xuan Zeng*

Homomorphic Encryption and Quantum Circuits Session

Session Code:	**B4L-06**	**Date & Time:**	**Tuesday May 26, 2026 (15:00 - 16:30)**
Location:	**3B**	**Chairs:**	**Xin Peng, Hanho Lee**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2545	3.8	Unified Architecture of Random Sampler for Fully Homomorphic Encryption *Muhammad Ogin Hasanuddin, Fajri Sachruddin, Hanho Lee*
1882	3.8	Memory-Efficient Twiddle Factor Generator in Parallel NTT Accelerators for FHE Applications *Gyuhyun Jung, Hyunhoon Lee, Youngjoo Lee*
1222	3.8	HyperNTT: An Ultra-High Throughput Number Theoretic Transform Accelerator for FHE *Yan Xu, Xiyan Dong, Jiarui Wang, Leyan Zhang, An Wang, Xinghua Wang, Liehuang Zhu, Jingqi Zhang*
2011	3.8	Design of a Compact QRNG in 22nm Standard CMOS Technology *Andrea Bonzi, Nicola Massari, Luca Parmesan, Fabio Acerbi, Sonia Mazzucchi, Aymane Bouzafour, Marc Renaudin, Leonardo Gasparini*
2119	3.8	Additive Resource Scaling in Quantum Circuits for Search in Cryptanalysis *Leonardo Lavagna, Giacomo Vittori, Antonello Rosato, Massimo Panella*

Circuits & Systems for Energy Harvesting I Session

Session Code:	**B4L-07**	**Date & Time:**	**Tuesday May 26, 2026 (15:00 - 16:30)**
Location:	**3G**	**Chair:**	**Junrui Liang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2001	4.5	A Dual-Path SSHC Rectifier with Decoupled Battery Architecture for Enhanced Piezoelectric Energy Harvesting *Jing Wang, Yi Yang, Zhen Li, Yixin Zhang, Jiafei Yao, Xiaoyang Zeng, Yufeng Guo*
2487	4.5	Piezoelectric Energy Harvesting Interface with High Frequency Mismatch Tolerance Based on a Novel Two-Dimensional MPPT Algorithm *Bo Qin, Min Sun, Haolu Xie, Xing Li*
2041	4.5	A Synchronous Switch Multi-Shot Energy Extraction Circuit for Electromagnetic Energy Harvesting *Le Cheng, Jiacong Qiu, Junrui Liang*
2347	4.5	A Photovoltaic Energy-Harvesting Chip Featuring Self-Adaptive-Monitoring-Time MPPT *Jiaqing Li, Wenjie Yang, Chenyang Tao, Changgui Yang, Kai Huang, Bo Zhao*
2538	4.5	A Self-Adaptive Digital Control with 20 ns Precision for Zero Current Switching for Next Generation TEG-Based Wearable Devices *Praveen Negi, Sumukha KS, Murali Krishna Rajendran*

Nanoelectronic Circuits Session

Session Code:	**B4L-08**	**Date & Time:**	**Tuesday May 26, 2026 (15:00 - 16:30)**
Location:	**5C**	**Chairs:**	**Feng Zhang, Georgios Ch. Sirakoulis**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1336	5.1	A Low-Power 2-Bit Full Adder Realized with Three-Independent-Gate Reconfigurable Fets *Giulio Galderisi, Yuxuan He, Juan Pedro Martinez, Niladri Bhattacharjee, Binit Syamal, Viktor Havel, Violetta Sessi, Thomas Mikolajick, Jens Trommer*
1718	5.4	A 454.9-kHz, 65,100-NAND2-Equivalent-Gate Flexible Cortex-M0 SoC in 3-μm LTPS TFT Technology *Jingkai Song, Anzhi Yan, Enyi Zhang, Houfang Liu, Yi Yang, Tian-Ling Ren*
1263	5.1	SPPA: A Self-Adaptive Pruning and Parallel Annealing Algorithm for Ising Computing *Wenya Deng, Zhi Wang, Yingzhe Luo, Junwei Zeng, Sheng Liu, Xiaowen Chen, Yang Guo*
2285	5.5	Hierarchical Fault Mitigation Architecture in Radiation-Hardened STT-MRAM *Yantong Di, Haoran Du, Yibo Liu, Huanghui Wang, Wen Wang, Jingchao Zhang, Chao Ma, Bo Liu, Hao Cai*
2472	5.10	Universal OMA Tracker Using Sampled Envelope Feedback for Wavelength Locking of High-Speed Micro-Ring Modulators *Yaowen Tu, Da Ming, Chengkun You, Min Tan*

Neuromorphic Processor Architecture and System Session

Session Code:	**B4L-09**	**Date & Time:**	**Tuesday May 26, 2026 (15:00 - 16:30)**
Location:	**5F**	**Chairs:**	**Yuncheng Lu, Xinming Shi**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2448	8.4	A Neuromorphic ASIC Design for Dexterous Hand Control *Hengtan Zhang, Zeyu Wang, Yifu Liang, Jie Lu, Li Gong, Zhongxue Gan, Li-Rong Zheng, Zhuo Zou*
2656	8.2	DyNeuro: A Hybrid Neuromorphic Accelerator with Dynamic Spatio-Temporal Variation Adaptations *Youming Yang, Yi Zhong, Li Lun, Tao Zhang, Xiaoxin Cui, Yuan Wang*
1969	8.4	nanoHEENS: Biomimetic Near-Memory-Computing 16-Core SIMD Processor Node for Evolutive Spiking Neural Networks *Arnau Larré Alòs, Bernardo Vallejo-Mancero, Víctor Torres, Daniel Fernández, Mireya Zapata, Joan Manuel Moreno, Jordi Cosp-Vilella, Jordi Madrenas*
1182	8.2	AURA: A Reconfigurable Asynchronous Spiking Processor for Low-Power Sensory Systems *Shimeng Ye, Stijn van Himste, Roel Jordans, Sander Stuijk, Federico Corradi*
1575	8.2	TSA-P: A Triple-Sparsity-Aware Reconfigurable Few-Spikes-Neuron-Based SNN Processor *Lin Tang, Aoyu Shen, Ruixin Mao, Bo Zhao, Jun Zhou*

Machine Learning for Signal Processing Session

Session Code:	**B4L-10**	**Date & Time:**	**Tuesday May 26, 2026 (15:00 - 16:30)**
Location:	**5D**	**Chairs:**	**Yudong Zhang, Xin Lou**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1268	10.8	An RTL-Based CNN Inference Module for Low-Power Edge Vision Applications *Chiang Liang Kok, Bofan Zhao, Jovan Bowen Heng, Liheng Lou, Xiwei Huang, Tee Hui Teo*
1708	10.8	UniOOD: A Unified Framework for Domain Generalization and Out-of-Distribution Detection in Time Series *Yongming Chen, Wenwen Zheng, Bah Hwee Gwee, Qi Cao, Sirajudeen Gulam Razul, Zhiping Lin*
1831	10.8	Patch Size-Considered Incremental Learning for Video Compression Artifact Reduction *Zhen Feng, Cheolkon Jung*
2057	10.8	CryHop: Baby Cry Classification on Dunstan Dataset Using Transfer Learning and Ensembling *Soheil Khooyooz, Loic Ricard, Jiayue Liu, Mostafa Haghi, Nima Taherinejad*
1952	6.8	A Wavelet-Enhanced Neural Network with Knowledge Distillation for MCU-Based Fingerprint Liveness Detection *Zhengwu Li, Kaixiang Lin, Xiaojin Zhao, Wenbin Ye*

Compute-in-Memory I Session

Session Code:	**B4L-11**	**Date & Time:**	**Tuesday May 26, 2026 (15:00 - 16:30)**
Location:	**5H**	**Chair:**	**Peilin Liu**

Papers are listed in the order they will be presented.

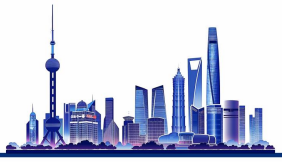
Paper Id	Topic	Title/Author
1005	14.1	STM-CIM: A 2427 TOPS/W Signed Compute-in-Memory with Analog-Domain Top-K and Matrix Transpose for CNN & Transformer *Xiaoya Wang, Tingran Chen, Xinyi Zhang, Shuo Liang, Yimin Yang, Weijie Ding, Biao Pan*
1050	14.1	A 0.58 Ops/Trans Analog Compute-in-Memory Macro with Input Operand Generator Supporting Wide Boolean Operations for Enhanced Versatility *Eun-Bi Koh, Jeong-Eun Ko, Joo-Hyung Chae*
1319	14.1	FABS-CIM: Unlocking A/D Conversion Bottlenecks of Bit-Serial Computing-in-Memory with Analog Shift-and-Addition and In-Situ Batch Normalization *Liang Zhang, Yang Liu, Junda Zhao, Jing Kou, Junzhan Liu, Wang Kang*
1418	14.1	A 28nm 143.4-322.5TOPS/W INT8 Time-Domain CIM Macro Featuring Zero-Weight Skipping and Shift-and-Add Embedded TDC for Deep Neural Network *Ao Shi, Yiyang Chen, Lianliang Wu, Jiaqi Li, Siyuan Chen, Haobin Shang, Ruiqi Chen, Nan Tang, Kexun Li, Lifeng Liu, Xiaoyan Liu, Jinfeng Kang, Peng Huang*
1646	14.1	VFE-CIM: An Algorithm-Hardware Co-Designed Computing-in-Memory Accelerator for Efficient Voxel Feature Encoding in Large-Scale Point Clouds *Yuang Ma, Shiyu Fan, Ziwei Li, Song Chen, Yi Kang*

Computational Intelligence for Multimedia Understanding Session

Session Code:	**B4L-12**	**Date & Time:**	**Tuesday May 26, 2026 (15:00 - 16:30)**
Location:	**5E**	**Chairs:**	**Maria Trocan, Behçet Uğur Töreyin**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1770	18.2	HalF&D: A Parameter Efficient Small Object Detection Approach *Ahmet Nuri Yilmaz, Onur Can Koyun, Behçet Uğur Töreyin*
1768	18.2	Comparison of Feature Selection Methods for High-Dimensional Small Datasets *Harald Rietdijk, Patricia Conde-Cespedes, Talko Dijkhuis, Hilbrand Oldenhuis, Maria Trocan*
1676	18.2	Residual-Free Image Reconstruction from HEVC for Compressed-Domain Visual Analytics *Muhammet Sebul Beratoğlu, Behçet Uğur Töreyin*
2378	18.2	Reliable and Trustworthy Learning Prototype: Insight from POCUS *Giacomo Ignesti, Gennaro D'Angelo, Lorenza Pratali, Davide Moroni, Massimo Martinelli*



Empowering the Evolving Electrical Grid: Circuits & Systems for Greener Generation, Distribution II Session

Session Code:	**B4L-13**	**Date & Time:**	**Tuesday May 26, 2026 (15:00 - 16:30)**
Location:	**5A**	**Chairs:**	**Federico Bizzarri, C. K. Michael Tse**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1236	15.9	Strategic Transmission Line Upgrades of Power Systems Under High Renewable Penetration *Meixuan Li, Chi Kong Tse, Cheng Zhu, Xianqiang Zhu*
1888	15.9	Robust Data-Driven Distributed Control Strategy for Dynamic Energy Scheduling in Hybrid Energy Systems *Wendong Feng, Chengyan Zheng, Xinan Zhang, Herbert Ho Ching Iu, Tyrone Fernando*
1053	15.9	High Performance Fault-Tolerant Control for DC-DC Buck-Boost Converters: An Unsupervised Learning-Based Approach *Mehdi Forouzanfar, Anna Pinnarelli, Hossein Safaeipour*
2138	15.9	Spatio-Temporal Power Flow Forecasting During Cascading Failure Propagation in Power Systems *Biwei Li, Dong Liu, Chi K. Tse, Junyuan Fang, Xi Zhang*

Sensing Interfaces and SoCs Session

Session Code:	**B4L-14**	**Date & Time:**	**Tuesday May 26, 2026 (15:00 - 16:30)**
Location:	**5B**	**Chairs:**	**Pantelis Georgiou, Changgui Yang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2222	6.8	A Low Noise Active Pixel Circuit Using Dual Correlated Double Sampling for Dynamic TFT Integrated X-Ray Imaging *Haotian Han, Weiming Yuan, Jiangbo Hu, Yuhan Zhang, Lu Chang, Xin Zheng, Congwei Liao, Shengdong Zhang*
2372	6.7	An Electrochemical Sensing SoC for Autonomous Wound Monitoring *Maxx Seminario, Seth McRobert, Ayden Uerling, Joseph Schmitz, Paige Aberson, Sina Balkir, Eric Markvicka*
2437	6.9	Design and Validation of a Clocked gm-C Bandpower Extraction Circuit for Biosignal Analysis *Jiaqi Ge, Vichaya Manatchinapisit, Berkay Özbek, Timothy Constandinou*
2766	6.6	A Miniaturized Wireless Multimodal Physiological In-Vivo Monitoring Platform Featuring Power-Efficient Photoelectrochemical Sensing *Zepeng Huang, Lifeng Yan, Wenxian Gu, Xing Wu, Liangjian Lyu*
2956	6.8	In-Pixel Decorrelation Time Approximation Circuit for Rapid Wide-Field Dynamic Light Scattering Imaging *Yining Wang, Robert Henderson*

RF and mm-Wave Transceivers and Receivers Session

Session Code:	**B5L-01**	**Date & Time:**	**Tuesday May 26, 2026 (16:30-18:00)**
Location:	**3C**	**Chairs:**	**Jerald Yoo, Arindam Sanyal**

Papers are listed in the order they will be presented.

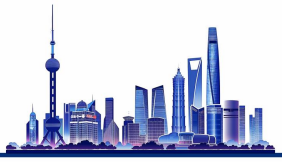
Paper Id	Topic	Title/Author
1100	1.2	An Ultra-Low-Power Energy-Harvesting Wireless Transmitter with Nanowatt Duty-Cycled Operation for Autonomous Sensor Networks *Seyyedmohsen Seyyedrezaei, Florian Protze, Jens Wagner, Frank Ellinger*
2612	1.2	An Ultra-Low-Power, High-Output-Power and High-Sensitivity Bioelectronic Transceiver *Ruohan Wang, Xiaoyuan Wu, Kangjie Zhao, Chunqi Shi, Leilei Huang, Jinghong Chen, Runxi Zhang*
1375	1.2	A 24-29.5-GHz Phased-Array Receiver with Sub-Degree RMS Phase Errors and Wide Gain Tuning Range in 130-nm SiGe BiCMOS *Kejie Hu, Kaixue Ma, Jiancheng Huang, Bing Liu, Xuguang Li, Yu Wang, Xu Wang, Zonglin Ma, Ningning Yan, Yongrong Shi*
1567	1.2	A Time-Division Multiplexing Dual-Band Self-Powered WuRX for WSNs *Shaohua Zhang, Yuyuan Wang, Yinuo Zhang, Xufeng Liao, Zhangming Zhu, Lianxi Liu*
1058	1.2	A Compact 0.2-19GHz Zero-IF Reconfigurable Quadrature Transmitter with Dual-Band Selection in 28nm CMOS Process *An Sun, Junjie Gu, Haoqi Qin, Weitao He, Yaxin Zeng, Hao Xu, Na Yan*

Noise-Shaping ADCs and DAC Techniques for SAR ADCs Session

Session Code:	**B5L-02**	**Date & Time:**	**Tuesday May 26, 2026 (16:30-18:00)**
Location:	**3I+3J**	**Chairs:**	**Luis Hernandez, Gonçalo Rodrigues**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2621	1.3	An Enhanced-Bandwidth Noise-Shaping SAR ADC Using RC-Tracking Circuit as Amplifier *Ziyuan Guo, Eric Christie, Yen-Cheng Kuan, Long Kong, Shiuh-hua Chiang*
1037	1.3	A Noise-Shaping SAR ADC with Second-Order Input Prediction *Viet Nguyen-Thien, Chadi Jabbour, Minh-Tien Nguyen, Nicolas Delorme*
2142	1.3	A Two-Stage Machine Learning Assisted Calibration Scheme Achieving 73.3dB SNDR and 87dB SFDR for a 14-Bit Pipelined NS-SAR ADC *Siqi Zhang, Jiaju Lu, Xinzhe Xie, Wang Ling Goh, Jinhai Hu, Yuan Gao*
2275	1.3	A Highly Linear SAR ADC Architecture with a Correction-Free Hybrid DAC *Yanquan Luo, Nan Sun*
2616	1.3	A Compact 18-Bit 1-MS/s SAR ADC Using Passive-Charge-Redistributed DAC *Liuxue Sun, Yiyang Wang, Haonan Huang, Yuke Shen, Yanbo Zhang, Yuhua Liang, Zhangming Zhu*



Advanced Analog and Mixed-Signal Techniques I Session

Session Code:	**B5L-03**	**Date & Time:**	**Tuesday May 26, 2026 (16:30-18:00)**
Location:	**3A**	**Chairs:**	**Randall Geiger, Ankesh Jain**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1082	1.8	A Low Power 0.45pJ/b, 5.4Gbps, Single Ended Next Generation Toggle NAND Flash Controller PHY with Boosted CTLE and Merged Transceiver *Ashish Savadia, Hanan Borukhov, Prashant Jaitly, Ajay Kumar, Gilad Marko, Ofir Zadik, Kishore Mindala, Gopikrishna Siddula, Utkarsh Srivastava, Srinivasamuni Adepu, Erez Frank, Ramakrishnan Subramanian*
1348	1.8	Three-Independent-Gate Reconfigurable Transistors in 22 nm FDSOI for In-Sensor Time-Domain Mixed-Signal Processing *Juan Pedro Martinez, Yuxuan He, Giulio Galderisi, Roberta Grasso, Marrit Jen Hong Li, Junyan Qian, Eugenio Cantatore, Sandro Carrara, Thomas Mikolajick, Jens Trommer*
2023	1.8	A Low-Power Fractional Output Divider with Adaptive Power Control Algorithm in 28-nm CMOS *Zhenze Yang, Chang Liu, Sheng Hu, Peipei Li, Xiao Ma, Bo Li*
2078	1.8	An Ultra Low-Power True Random Number Generator for RFID Systems in 65 nm CMOS *Luis Esteban Hernández, Carlos Saccogna, Vladimir Milovanović*
1364	1.6	A Compact-Area Digital-Output CMOS Test Module for Random Telegraph Noise Characterization *Juan Campoverde, Javier Cuenca-Michans, Pol Comas, Guido Janssen, Roy Starr, Lluís Terés, Francisco Serra-Graells*

Hardware Security for Logic, Circuits and Architectures III Session

Session Code:	**B5L-04**	**Date & Time:**	**Tuesday May 26, 2026 (16:30-18:00)**
Location:	**3D**	**Chairs:**	**Xiaojin Zhao, Chi-Chia Sun**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2821	2.7	GUARDIAN: A Decoupled GNN Framework for Type-Aware Hardware Trojan Detection *Zain Shabbir, Shichao Yu, Ihsen Alouani, Maire O'Neill*
2843	2.7	TRACEFORMER: Trace-Efficient and Robust Transformer-Based Late-Fusion Side-Channel Analysis of Masked AES *Ali Alper Sakar, Elif Bilge Kavun*
2847	2.7	Power Side-Channel Attacks in Nanosheet Circuits *Mohammed Nabeel, Hadi Nour Eddine, Mahdi Benkhelifa, Ozgur Sinanoglu, Michail Maniatakos, Johann Knechtel, Hussam Amrouch*
2939	2.4	A SAW-Less Low-Noise Spread-Time CDMA Low-IF Receiver for IoT Applications *Roham Ahmadvand, Mohammad Hossein Tazari, Nima Dehghan, Fatemeh Akbar, Mohammad Amir Dastgheib, Jawad A. Salehi*

Programmable, Reconfigurable & Array Architectures I Session

Session Code:	**B5L-05**	**Date & Time:**	**Tuesday May 26, 2026 (16:30-18:00)**
Location:	**3E**	**Chairs:**	**Danella Zhao, Chung-An Shen**

Papers are listed in the order they will be presented.

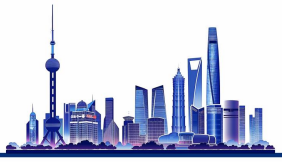
Paper Id	Topic	Title/Author
1061	2.5	RL-FRA: Exploration and Optimization of FPGA Routing Architectures via Model-Based Reinforcement Learning *Yuanqi Wang, Xianfeng Cao, Lingli Wang*
1332	2.5	MOE: An Efficient Multicasting and One-Hot Encoding Hybrid Configuration Compression Technique for CGRAs *Hanyu Zhang, Yuan Dai, Wenbo Yin, Lingli Wang*
1554	2.5	SNTT: A Sparsity-Aware NTT Accelerator Based on FPGA for Zero-Knowledge Proof *Zihang Guo, Qiang Liu, Ray C.C. Cheung, Zhaohui Guo*
1590	2.5	A 22nm Reconfigurable Systolic Array for FFT and AI Inference *John Stolzberg-Schray, Sharad Nag, Jacob Johnson, Nikhil Kumar Cherukuri, Ashish Kumar Kola, Gopikrishnan Raveendran Nair, Jeff Zhang, Jae-Sun Seo, Yu Cao*
1825	2.5	IDSPfree: An FPGA-Based Intrusion Detection System with DSP-Free Design *Abdessamad Nassihi, Ahmed Sadaqa, Muhammad Iqbal Khan, Han Bao, Ruiqi Chen, Bruno Da Silva*

AI/ML for Communication and Signal Processing Session

Session Code:	**B5L-06**	**Date & Time:**	**Tuesday May 26, 2026 (16:30-18:00)**
Location:	**3B**	**Chairs:**	**Youngmin Kim, Shan Cao**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1867	3.6	MeritFL: Self-Regulating Federated Learning via Merit-Gated Communication *Zhengliang Guo, Kun Yang, Linxiao Gong, Yang Liu, Jing Liu, Liang Song*
2215	3.10	MANBO: A Multi-Agents PPO Network-Based Optimizer Framework for Multi-Operand Adders *Yan Tian, Jienan Chen*
2358	3.1	Fast and Accurate SystemVerilog Framework for Mixed-Signal Modeling of PAM-4 Wireline Transceivers *Yujin Choi, Seongjin Kim, Seoyoung Jang, Donggeon Kim, Korkut Kaan Tokgoz, Gain Kim*
2079	3.6	A ML-Based Robust Channel Estimation Enhancer Against Multi-Tone Jamming in OFDM Systems *Chaofan Deng, Ashwin Bhat, Adou Sangbone J Assoa, Katarina Vuckovic, Subbhashish Chakravarty, Arijit Raychowdhury*



Circuits & Systems for Energy Harvesting II Session

Session Code:	**B5L-07**	**Date & Time:**	**Tuesday May 26, 2026 (16:30-18:00)**
Location:	**3G**	**Chair:**	**Junrui Liang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1653	4.5	A ReMOS Cross-Coupled Charge Pump Achieving 0.62-V VDR and 81.5% Peak PCE for Micro Energy Harvesting Applications *Adrian Jie Ern Lim, Harikrishnan Ramiah, Yi Khang Ooi, Kishore Kumar Pakkirisami Churchill, Andrea Ballo, Yong Chen*
1981	4.5	A 915MHz Wide-Input Range CMOS Rectifier with Variable Common-Mode Feedback Achieving 75.2% Peak Efficiency *Jinzhe Qin, Simeng Yin, Peidong Chen, Kaixue Ma, Keping Wang*
2322	4.5	A Compact Wide-Band RF Energy Harvesting Front-End Based on an On-Chip IMN with 51.78% Peak PCE *Zushuai Xie, Ying Zhou, Guoqing Li, Tinghuan Chen, Zhikuang Cai, Zixuan Wang*
2693	4.5	A 0.3-nA Quiescent Current CMOS-Only Undervoltage Lockout Circuit with Dual-Mode Operation for Energy Harvesting Systems *Raghav Bansal, Sanjeev Kumar, Shouri Chatterjee*
1923	4.5	An Adaptive Sampling Frequency FOCV MPPT Based on Energy-Packet-Counting for Energy Harvesting Applications *Youlin Wu, Chenchang Zhan, Huajun Guo, Zhen Wang*

Quantum Computing II Session

Session Code:	**B5L-08**	**Date & Time:**	**Tuesday May 26, 2026 (16:30-18:00)**
Location:	**5C**	**Chairs:**	**Hao Cai, Feng Zhang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1170	5.7	A Fewer-Cycles, Resource-Efficient Concurrent Calibration Method for Compact Transmon Qubit Control and Readout Circuit *Heyue Li, Qichun Liu, Yanshu Guo, Tiefu Li, Zhihua Wang, Hanjun Jiang*
1184	5.7	Power Delivery for Cryogenic Scalable Quantum Applications: Challenges and Opportunities *Yating Zou, Batuhan Keskin, Gregor Taylor, Zenghui Li, Jie Wang, Eduard Alarcón, Fabio Sebastiano, Masoud Babaie, Edoardo Charbon*
1249	5.7	A Digital Baseband ASIC Targeting 99.999% Fidelity for Qubit Control and Readout with ROI-Based Classification *Heyue Li, Siqi Zhang, Tian Tian, Guo Wei, Yaoyu Li, Yanshu Guo, Tiefu Li, Zhihua Wang, Hanjun Jiang*
1850	5.7	A Power Efficient and Fast Response Cascode FVF LDO Using Voltage Detecting and GB Enhancing Techniques for Cryogenic Quantum Computing *Chengzhuo Zhao, Mingche Lai, Fangxu Lv, Weixia Xu, Heng Huang, Kewei Xin, Wenchen Wang, Meng Li, Chaolong Xu, Jiliang Liu*
2718	15.15	AA Monolithic 5×14-Channel Cryo-CMOS Multiplexer for Scalable Control of Trapped-Ion Qubits *Xuefeng Liu, Fuyi Li, Zhiyun Zhang, Peng Xiao, Yongfu Li, Bo Li, Yong Wang, Xiaoxi Li, Xiguang Wu, Wei Mao, Yan Liu, Genquan Han*

Neuromorphic Learning and Plasticity Session

Session Code:	**B5L-09**	**Date & Time:**	**Tuesday May 26, 2026 (16:30-18:00)**
Location:	**5F**	**Chair:**	**Qinyu Chen**

Papers are listed in the order they will be presented.

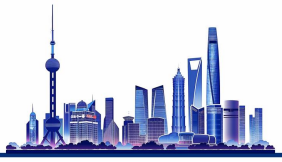
Paper Id	Topic	Title/Author
1634	8.2	GreenMorph: Sustainable Neuromorphic Computing Through Energy-Harvesting and Energy-Driven Online STDP Learning *Yuga Hanyu, Subbaiah Ravi Hariprakash, Abderazek Ben Abdallah, Zhishang Wang, Khanh Dang*
1916	8.2	Mixed-Signal Implementation of Feedback-Control Optimizer for Single-Layer Spiking Neural Networks *Jonathan Haag, Christian Metzner, Dmitrii Zendrikov, Giacomo Indiveri, Benjamin Grewe, Chiara De Luca, Matteo Saponati*
2342	8.2	Hardware-Aware Attractor Dynamics in Neuromorphic Systems: Compensating for Device Mismatch Through Network Design *Leonardo Martinelli, Chiara De Luca, Giacomo Indiveri*
1946	8.8	Implementation of Spike-Timing-Dependent Plasticity for Epileptic Seizure Recovery on Neuromorphic Memristive Hardware *Iván Díez-De-Los-Ríos, Luis Camuñas-Mesa, Teresa Serrano-Gotarredona, Bernabé Linares-Barranco*
2528	8.2	Enhancing Neuromorphic Pattern Selectivity for Imbalanced Data by Adapting from Homeostasis *Luke McCarthy, Ben Walters, Amirali Amirsoleimani, Mostafa Rahimi Azghadi*

Signal Processing Theories and Algorithms for Biosignals Session

Session Code:	**B5L-10**	**Date & Time:**	**Tuesday May 26, 2026 (16:30-18:00)**
Location:	**5D**	**Chair:**	**Wei Liu**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1044	10.11	Towards Practical Reliability Assessment of RF-Based Heartbeat Sensing with Multi-Domain Analysis *Hanqin Gong, Yadong Li, Jiahao Xu, Jinbo Chen, Dongheng Zhang, Yang Hu, Yan Chen*
1639	10.11	Identification of ADHD Biological Subtypes with Variational Autoencoder Network *Yuan Gao, Jiahao Gao, Yibin Tang, Ying Chen, Chun Wang*
1896	10.11	Discrete High-Gain Observer Based Epileptic Seizure Prediction by Single-Lead ECG *Dinghan Hu, Tiejia Jiang, Tianyang Chen, Jiuwen Cao*
2968	10.11	A Neural Spike Sorting Framework with Multi-Scale Slope Detection and Lite-CNN Classification *Yulun Peng, Wenxian Gu, Jingjie Tang, Lifeng Yan, Xing Wu, Liangjian Lyu*



Compute-in-Memory II Session

Session Code:	**B5L-11**	**Date & Time:**	**Tuesday May 26, 2026 (16:30-18:00)**
Location:	**5H**	**Chair:**	**Kannaujiya Aryan**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1760	14.1	DirectGeMM: Eliminating the GeMV Bottleneck in Analog In-Memory Computing *Tomohisa Kawakami, Tergel Molom-Ochir, Xudong Zhuang, Jiahui Yang, Tania Roy, Hai Li, Yiran Chen*
1790	14.1	An IZO-Based 2T0C Compute-in-Memory Array with Adaptive Read Voltage Boosting for Energy-Efficient Edge AI *Hao Ding, Jiye Li, Xiantong Qiu, Yunfan Yang, Gaoqi Yang, Jingwei Sun, Lei Lu, Shengdong Zhang, Zongwei Wang, Yimao Cai*
2014	14.1	Delta-Sigma Modulator-Based Compute-in-Memory Neural Network with Analog Feature Extraction and Classification for Edge Sensors *Tushar Gupta, Vasundhara Damodaran, Yuan Liao, Jae-Sun Seo, Arindam Sanyal*
2164	14.1	Horizontal-Parallel ADC-Less Sparsity-Clock-Aware RRAM CIM Macro for Edge AI Devices *Teng Zou, Shengchao Zhou, Hongrui Meng, Yufeng Xie*
2891	14.1	Energy-Efficient All-Digital Computation-in-Memory Macro Design with CFeFET-Based Booth Decoder *Ting-Wei Yang, Wei Lu, Yuan-Yu Huang, Pin Su, Po-Tsang Huang*

Circuits and Systems for Coding and Processing Session

Session Code:	**B5L-12**	**Date & Time:**	**Tuesday May 26, 2026 (16:30-18:00)**
Location:	**5E**	**Chair:**	**Heming Sun**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1329	11.14	HLC: A High-Quality Lightweight Mezzanine Codec Featuring High-Throughput Palette *Chenlong He, Leilei Huang, Wei Li, Hanyan Cui, Zhijian Hao, Xiaoyang Zeng, Yibo Fan*
1585	11.14	An Area-Latency-Balanced Hardware Design for the Reference Pixel Management of VVC Intra Coding *Chengkang Huang, Leilei Huang, Taoyu Zhang, Shuocheng Wang, Yibo Fan*
2784	11.2	Energy-Efficient Neural Video Coding via a High-Throughput Hardware Design for Pointwise Convolution and LUT-Based WSiLU *Denis Maass, Vanessa Aldrighi, Ruhan Conceição, Wen-Hsiao Peng, Luciano Agostini, Marcelo Porto*
2053	11.14	ERSRP: A 55nm 46.28 MPixels/(s·mm²) 104 FPS Efficient Real-Time Super-Resolution Processor with Layer-Fused Lightweight Engine *Gaoxiang Wu, Liang Chang, Jingke Wang, Jiahao Zeng, Zhicheng Hu, Xin Zhao, Liang Zhou, Fengbin Tu, Jun Zhou*
2390	11.2	Hardware-Friendly Machine-Learning-Based Fast AV1 Overlapped Block Motion Compensation *William Kolodziejski, Leonardo Braga, Marcelo Porto, Luciano Agostini*

Specialized Hardware for Embodied AI Application and Neuromorphic Computing I Session

Session Code:	**B5L-13**	**Date & Time:**	**Tuesday May 26, 2026 (16:30-18:00)**
Location:	**5A**	**Chairs:**	**Yueting Li, Bo Li**

Papers are listed in the order they will be presented.

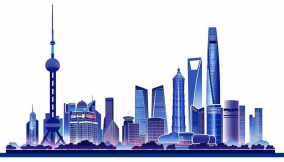
Paper Id	Topic	Title/Author
2132	15.13	Efficient LLM Inference on ARM via Hardware-Aware Operator Co-Design and Heuristic Mixed-Precision Search *Zhaode Wang, Jin Yao, Cheng Zhang, Shirui Zhao, Yong Wang, Xiaoxi Li, Xiguang Wu, Bo Li, Wei Mao, Yan Liu, Genquan Han*
1800	15.13	A Heterogeneous Decision Spiking Transformer Accelerator with Locality-Dependent KV Product Cache and Compute Pattern Reconfigurable Engine *Ziyang Shen, Zhipeng Liao, Sitan Shen, Chaoming Fang, Fengshi Tian, Jie Yang, Mohamad Sawan*
1691	15.13	A Pipelined NoC-Based Membrane Shortcut SNN Architecture for Low-Latency Spike Sorting *Jingsong Zhang, Yiwen Zhu, Fangduo Zhu, Chenyang Li, Siyuan Ouyang, Jinhao Liang, Jingyi Chen, Xumeng Zhang, Qi Liu*
1723	15.13	A Low-Power Resonate-and-Fire Neuron with Adaptive Refractory Control for RRAM-Based Neuromorphic Computing *Xucheng Yong, Ruiqi Ma, Tianze Wu, Ruolun Li, Yanze Xu, Zhichao Tan, Liang Zhao*
1510	15.13	Neural Quantization-Aware Piecewise Linear Approximation for Nonlinear Functions on FPGA *Fanhong Zeng, Chao Li, Runhan Li, Juntao Guan, Rui Lai, Zhangming Zhu*

Wireless Power and Implantable Systems Session

Session Code:	**B5L-14**	**Date & Time:**	**Tuesday May 26, 2026 (16:30-18:00)**
Location:	**5B**	**Chairs:**	**Arindam Basu, Hanjun Jiang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1127	6.6	TAuC-SoC: A 0.36 mm² In-Yarn Integrable Tiny Audio Compressor SoC for E-Textile Based Audio Recording Applications *Suprio Bhattacharya, Charles Hess, Omar Faruqe, J. Keith McElveen, Douglas Cairns, Doug Overland, Jonathan Johnson, Daniel Truesdell, Benton Calhoun*
1219	6.2	A Smart Rotation-Tolerant and Self-Positioning WPT System for Freely Moving Small Animals *Saeideh Pahlavan, Shahin Jafarabadi-Ashtiani, Seyed Abdollah Mirbozorgi, Mostafa Shooshtari, Teresa Serrano-Gotarredona, Bernabé Linares-Barranco*
2249	6.2	A Low-Power PWM-ASK Receiver Supporting High Supply Variation Tolerance and High Order Modulation for Wireless Implantable Applications *Jungwon Kwun, Jaeeun Jang*
2752	6.2	Design of a Wireless Power and Data Transfer System with Multi-Output Adaptive Rectifier and Harmonic Communication for Cochlear Implants *Kim-Hoang Nguyen, Quang Nguyen, Duy-Minh Nguyen, Soon-Jae Kweon, Loan Pham-Nguyen, Hanh-Phuc Le, Minkyu Je*
2398	6.6	BrainRead: Multi-Sensor Earable System for Continuous Physiological Sensing *Gitesh Kulkarni, Amagond Biradar, Adarsh A, Ullas Pradhan, Pradeep Kumar G, Shivam Gupta, Jhanavi R, Pallavi L S, Ashutosh Menon, Adikiran S B, Kiran Rudramuni, Arpan Pal, Jayavardhana Gubbi*



RF and mm-Wave Power Amplifiers and Combiner Session

Session Code:	C2L-01	Date & Time:	Wednesday May 27, 2026 (10:30 - 12:00)
Location:	3C	Chairs:	Luis Oliveira, Raafat Labadibi

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2161	1.2	A D-Band Power Amplifier with a Novel Gain-Boosting Structure Achieving 15.8-dB Gain and 23.9-GHz Bandwidth in 65-nm CMOS *Rui Han, Li Wang, Zunsong Yang, Yunbo Huang, Xiaoyu Shan, Zhijian Chen, Bo Li*
1225	1.2	A 30.4 dB Dynamic Range Pulse-Modulated Class-E RF PA with 11-Bit Digital Pulse Modulation Unit Achieving 25.3 dBm PSAT and 32.3% Peak PAE *Merkourios Katsimpris, Thomas Burger, Hua Wang*
2183	1.2	Performance-Reconfigurable Multi-Mode Doherty Power Amplifier Using Bias-Space Control *Siddharth Thakur, Mir Mohammad Shayoub, Yogesh Singh Chauhan, Nagaditya Poluri*
1823	1.2	A Fully-Differential Wideband Configurable Power Combiner and Splitter in 28-nm Bulk CMOS *Feiyang Xu, Tao Yuan, Hongtao Xu, Yun Yin*
1974	1.2	A 24.5-29.5GHz Active Bidirectional Phase Shifter with Impedance-Invariant Vector Modulation Achieving 0.29°-1.4° RMS Phase Errors *Ruida Li, Qingzhe Zhang, Kaixue Ma, Keping Wang*

SAR ADC Calibration and Energy Optimization Session

Session Code:	C2L-02	Date & Time:	Wednesday May 27, 2026 (10:30 - 12:00)
Location:	3I+3J	Chairs:	Edoardo Bonizzoni, Sohmyung Ha

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2765	1.3	A 90.8dB SNDR SAR ADC with a Mutual Calibration Scheme for Capacitor Array and a Dynamic-Biased Comparator *Wei Xu, Qian Lu, Zhiwei Wu, Dandan Zheng, Xiubin Jiang, Shiwei Wang, Kai Huang, Shuang Song*
2682	1.3	A 16-Bit SAR ADC with Auxiliary-Calibration-Capacitor Enhanced Digital Foreground Calibration *Xiao Wang, Siyuan Huang, Deng Luo, Ming Tao, Jianjun Chen, Yaqing Chi, Guofang Yu, Bin Liang*
2048	1.3	Optimizing the Energy Efficiency in SAR ADCs with Linear/Exponential Comparator Biasing *Nishan Chettri, Antonio Aprile, Calogero Marco Ippolito, Giuseppe Bruno, Edoardo Bonizzoni, Piero Malcovati*
2703	1.3	A 2-GS/s 6-Bit 2B/conv. Single-Channel SAR ADC with Comparator Offset Calibration in 28-nm CMOS *Giyoon Lee, Yigi Kwon, Byounghan Min, Dooyeoun Kim, Jihyun Kim*
1557	1.3	Exploration of a Multi-Bit TDC-Based PLL-SAR ADC with Dynamic Settling *Ahmed AbdelRahman, Amartya Basak, Runpeng Gao, Aniruddha Sriram, Un-Ku Moon*

Advanced Analog and Mixed-Signal Techniques II Session

Session Code:	**C2L-03**	**Date & Time:**	**Wednesday May 27, 2026 (10:30 - 12:00)**
Location:	**3A**	**Chairs:**	**Joseph Chang, Vanessa Chen**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1959	1.1	Frequency Channelized Filtering by Aliasing *Anmol Krishen Kachroo, Sudhakar Pamarti*
2831	1.2	Automatic Tuning of Effective “On” Resistance of Switches in N-Path Filters *Pankaj Rahi, Mayank Anupam, Imon Mondal*
2908	1.2	A 2-18GHz Tunable Bandpass Filter with Dual-Path Transformer Technique for Ultra-Wideband Applications *Kai Yang, Xin An, Yunjie Zhao, Borun Li, Tao Zhang, Qijun Lu, Bowen Wang, Zhangming Zhu*
2509	1.8	Discrete-Time Current Integrator in 65 nm CMOS as Analogue Electro-Optical Interface for an Optical Neural Network *Lukas Hüssen, Muh-Dey Wei, Arka Dipta Das, Dennis Raffauf, Jeremy Witzens, Renato Negra*
1748	1.8	Subharmonic to Superharmonic Optical Injection Locking of Ring Oscillators in Standard CMOS *Tejus Rao, Nicholas Vitale, Arjang Hassibi, Thomas Lee*

Low-Power Logic, Circuits & Architectures I Session

Session Code:	**C2L-04**	**Date & Time:**	**Wednesday May 27, 2026 (10:30 - 12:00)**
Location:	**3D**	**Chairs:**	**Yuan Du, Chung-An Shen**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1041	2.2	An Energy-Efficient 0.56-pJ/Cycle AVFS System Based on a Fast Transient Response Digital LDO and a Self-Calibrating Elastic Clock *Jiliang Liu, Zhengbin Pang, Fangxu Lv, Shijie Li, Jiaqing Xu, Qiang Wang, Lizhou Wu, Chengzhuo Zhao, Mingche Lai*
1367	2.2	A Compact Low-Voltage and Low-Power Flip-Flop with Static, Contention-Free, and Redundant-Transition-Free Operation *Suna Lee, Taegun Yim, Choongkeun Lee, Hongil Yoon*
1459	2.2	Perception-Core: Reconfigurable Energy-Efficient Domain-Specific Architecture with Multimodal Fusion for AIoT *Xinyu Wang, Yulong Li, Yang Xiang, Yuanhua Deng, Haixiang Ren, Hui Chen, Yuxiang Fu, Li Li*
1975	2.2	TNNSAT: A Tree-NN Based Small-Footprint ASR Processor with Scene-Adaptive On-Chip Training *Ningyuan Li, Weixuan Wang, Peng Zheng, Shun Zhang, Zhichen Zhang, Zhixuan Gong, Zhen Wang, Bo Liu*
2064	2.2	Efficient VLSI Architecture for Finding Maximum Value and its Corresponding Index *Jayarani Medakal Anirudhan, C V Tirumala Rao, Subrahmanyam Mula*

Design and Verification of Digital Integrated Circuits and Systems I Session

Session Code:	**C2L-05**	**Date & Time:**	**Wednesday May 27, 2026 (10:30 - 12:00)**
Location:	**3E**	**Chairs:**	**Tian-Sheuan Chang, Meiqi Wang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1132	2.10	A Double-Node-Upset Tolerant Latch for Enhanced Reliability in Radiation-Prone Environments *Zijie Gong, Jilong Zhang, Hongkai Zheng, Fuyuan Lang, Boyun Zhang, Yan Li, Xiaoyang Zeng*
1143	2.10	Boosting Vector Instruction Throughput in RISC-V via a Hybrid Decoupled Architecture with VLIW-Driven Execution *Weiying Wang, Qingchen Zhai, Ruozhou Xiao, Zhiwei Zhang*
1215	2.10	VERIMLA: A Unified Framework for Verilog Generation via Multi-Level Alignment and Formal Equivalence Verification *Wing W. Y. Ng, Jiale Chen, Jiayi Zhang, Wen Li, Meihua Liu*
1574	2.10	RTCore: A RISC-V Processor Featuring Nested Hardware Loop Optimization for Real-Time Control System *Qingchen Zhai, Weiying Wang, Yueyue Wang, Yuanyang Xiang, Chen Xu, Kunyu Zong, Ruozhou Xiao, Zhiwei Zhang*
1371	2.10	SVVHD: An Open-Source and Self-Verified Benchmark Framework for LLM Evaluation in VHDL Code Generation *Jiayi Zhang, Yan Huang, Jiale Chen, Meihua Liu*

CAS Education and Outreach and the Open Silicon Initiative Session

Session Code:	**C2L-06**	**Date & Time:**	**Wednesday May 27, 2026 (10:30 - 12:00)**
Location:	**3B**	**Chairs:**	**Ljiljana Trajkovic, Ibrahim Elfadel**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
3014	15.16	Toward Generative Silicon: The Next Frontier in Open-Source and AI-Driven Analog Design *Mehdi Saligane, Anhang Li, Saptarshi Ghosh, Boris Murmann*
2846	15.16	Open and Accessible Workflows for the Education and Prototyping of Nanoelectronic Devices *Georgios Kleitsiotis, Pantelis Fraidakis, Emmanouil Stavroulakis, Iosif-Angelos Fyrigos, Ioannis Vourkas, Malgorzata Chrzanowska-Jeske, Jin-Woo Kim, Georgios Ch. Sirakoulis*
1903	13.2	The Hacker Fab: An Open-Source Initiative for Nanofabrication Education *Joel Gonzalez, Yanbing Chen, Jay Kunselman, John Wirant, Elio Bourcart, Matthew Moneck, Tathagata Srimani, Larry Pileggi*
1447	13.3	A 3-Day ASIC Design Hands-On with the Minimal Fab *Hideharu Amano, Atsutake Kosuge, Hirofumi Sumi, Naonobu Shimamoto, Yukinori Ochiai, Yurie Inoue, Tohru Mogami, Yoshio Mita, Makoto Ikeda*
1816	13.3	From RTL to Prompt Coding: Empowering the Next Generation of Chip Designers Through LLMs *Lukas Krupp, Matthew Venn, Norbert Wehn*

Modeling, Control, and Power Management Session

Session Code:	**C2L-07**	**Date & Time:**	**Wednesday May 27, 2026 (10:30 - 12:00)**
Location:	**3G**	**Chairs:**	**Zhen Li, Federico Bizzarri**

Papers are listed in the order they will be presented.

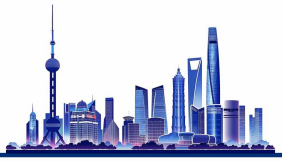
Paper Id	Topic	Title/Author
1151	4.10	Fast Frequency Response of Distribution Feeders Equipped with CIGs: An MRAC Based Approach *Farahnaz Ahmadi, Angelo Maurizio Brambilla, Davide Del Giudice, Federico Bizzarri*
2042	4.10	Uncertainty-Aware H2 Control of a Wave Energy Converter Prototype *Josefredo Silva, Marcio Lacerda, Erivelton Nepomuceno*
1849	4.12	A Capacitor-Less Current-Feedback LDO with Mismatch Cancellation Using DEM and Chopping for Distributed Power Management *Chengzhuo Zhao, Mingche Lai, Fangxu Lv, Jiaqing Xu, Xingyun Qi, Weixia Xu, Kewei Xin, Wenchen Wang, Jiliang Liu, Zhenyang Zhang*
2171	4.12	Ultra Low-Power CMOS Voltage References Designed with Automated Flow *Michele Caselli, Giorgio Bersani, Andrea Boni*
2230	4.12	Hardware and Software Collaborative Energy Management for a Light-Powered E-Ink Display *Jintao Meng, Jiacong Qiu, Junrui Liang*

WF-IoT Session

Session Code:	**C2L-08**	**Date & Time:**	**Wednesday May 27, 2026 (10:30 - 12:00)**
Location:	**5C**	**Chairs:**	**Hui Zhang, Bo Zhao**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2875	18.3	A 1.6-3.8 GHz Reconfigurable Transmitter with 81.5% Relative-Bandwidth PLL for FMCW Through-Wall Radar Applications *Yunqi Yang, Fanxun Cai, Ziyang Li, Pengcheng Wang, Yilin Xu, Junkai Jiao, Hui Zhang*
2668	18.3	A Low-Cost Subtractive Dither for Continuous-Time 1-Bit Delta-Sigma Modulators *Yilin Xu, Yiqin Chen, Renjie Fu, Linxu Shi, Zhigang Fu, Shixuan Wang, Hui Zhang*
2262	18.3	A 74.5-dB DR 1.25-MHz BW Continuous-Time Delta-Sigma ADC Using Low-Noise Feedback DAC with Optimized Barrel Shifter *Zhigang Fu, Renjie Fu, Linxu Shi, Yilin Xu, Deming Zhang, Hui Zhang*
2496	18.3	MEPUF: A Lightweight and ML-Resistant Strong PUF Integrating Dual-Mode MRAM and Configurable AES for Reliable UAVs *Jiaxin Li, Bi Wang, Yan Qiao, Luyao Shi, Chao Wang, Zhaohao Wang*
2686	18.3	Characterization of Silicon-Germanium Heterojunction Bipolar Transistor from Cryogenic to High Temperatures for Extreme Environment Applications *Xiaodi Jin, Hao Lei, Hao Su, Yongchen Wang, Fanxun Cai, Xiao Fang, Hui Zhang, Yatao Peng*



Hardware-Aware Neural Networks Session

Session Code:	**C2L-09**	**Date & Time:**	**Wednesday May 27, 2026 (10:30 - 12:00)**
Location:	**5F**	**Chairs:**	**Chang Gao, Hui Chen**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2159	8.3	An Isomorphic Transformation for Hardware Implemented Non-Negative Neural Networks *Manos Kirtas, Nikolaos Passalis, Nikos Pleros, Anastasios Tefas*
2196	8.1	SLaB: Sparse-Lowrank-Binary Decomposition for Efficient Large Language Models *Ziwei Li, Yuang Ma, Yi Kang*
2382	8.1	harDyT: A Post-Training Hardware-Aware Layernorm Replacement *Lubin Gauthier, Francis Bony, Julien Perchoux*
2479	8.1	Dynamic Phased Pruning with Similarity-Aware Filter Selection *Yingxian Jiang, Yaoyao Yan, Feiyue Diao, Fei Wang, Weizhi Xu, Hui Yu*
2486	8.1	PipeInfer: A Pipelined Inference Framework for U-Net Like Neural Networks *Chujun Feng, Congyu Lin, Xiaoying Zheng, Yongxin Zhu*

Image Processing: Segmentation, Compression, Restoration, Registration, and Enhancement Session

Session Code:	**C2L-10**	**Date & Time:**	**Wednesday May 27, 2026 (10:30 - 12:00)**
Location:	**5D**	**Chairs:**	**Qing Shen, Izzet Kale**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1059	10.10	PathDiff: Efficient Patch-Level Histology Image Synthesis with Pathology-Prior Guided Diffusion *Yixuan Dong, Fang-Yi Su, Jinwen Xu, Fuji Yang, Bingo Wing-Kuen Ling*
1062	10.10	Debiasing Diffusion Model: Enhancing Fairness Through Latent Representation Learning in Stable Diffusion Model *Lin-Chun Huang, Yixuan Dong, Fang-Yi Su, Ching Chieh Tsao, Fuji Yang, Bingo Wing-Kuen Ling*
1563	10.10	Variable-Rate Learned Image Compression Using Parameter Efficient Fine-Tuning and Trainable Quantization Step-Size *Ran Wang, Yongqiang Wang, Heming Sun, Jiro Katto*
1827	10.10	LLIENet: Generative Low-Light Image Enhancement Network Based on Retinex Theory *Lu Liu, Cheolkon Jung*

Conventional and Emerging Memory Circuits and Architectures Session

Session Code:	**C2L-11**	**Date & Time:**	**Wednesday May 27, 2026 (10:30 - 12:00)**
Location:	**5H**	**Chair:**	**Ettore Napoli**

Papers are listed in the order they will be presented.

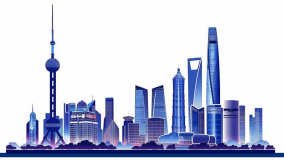
Paper Id	Topic	Title/Author
1380	14.1	A 0.277pW/Bit Sleep 10T SRAM with Improved Read/Write SNM for Low Leakage Applications *Xiang Li, Pengyuan Zhao, Minglong Jia, Linnan Li, Huidong Zhao, Xiaoqin Wang, Shushan Qiao*
1588	14.1	PSVS: A Parallel–Series Voltage-Sensing 1T4R RRAM Macro Achieving 15-Level Storage and 17.88 Mb/mm² Density for LLM Inference *Kaijun Zhang, Wencong Wu, Peizhe Li, Jiapei Zheng, Jinru Lai, Xiaoxin Xu, Qi Liu, Chixiao Chen*
1635	14.1	Asymmetric Read Transistor Configuration Enabled Low-Power 2T0C CAA-AOSFET Crossbar Array Through Sneak Current Suppression *Zhibin Zhang, Yecheng Yang, Shao Hao Wang*
1945	14.1	DS-eDRAM: Mode-Adaptive Dynamic-Static 2T-1C HZO eDRAM with Temperature-Aware Operation and Shared-Path Sensing for Energy-Efficient SPM in AI Accelerators *Ruijun Lin, Taoran Shen, Ruicong Zhang, Jie Yin, Li Xiong, Ming Wang, Xiaoyong Xue, Xiaoyang Zeng*
2492	14.1	A 1.8-ns, 45fJ/Bit Time-Domain Sensing Scheme with Offset-Cancelled Resistance-to-Time Converter and 10-5 BER for Digital RRAM Compute-in-Memory *Shigeng Zhao, Hao Ding, Yunfan Yang, Jinshan Li, Zhuoya Chen, Xing Zhang, Zongwei Wang, Yimao Cai*

Video Coding Session

Session Code:	**C2L-12**	**Date & Time:**	**Wednesday May 27, 2026 (10:30 - 12:00)**
Location:	**5E**	**Chair:**	**Li Li**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2163	11.1	Accelerating Entropy Coding via Probability State Caching Mechanism (PSCM) *Yufan Chen, Jiahao Liu, Lu Yu*
1979	11.1	Enhanced RDOQ for Dependent Quantization in VVC *Jiahao Liu, Yufan Chen, Lu Yu*
2981	11.1	Adaptive Resolution and Chroma Subsampling for Energy-Efficient Video Coding *Amritha Premkumar, Christian Herglotz*
2038	11.1	Standard-Compliant Joint Optimization of Rate-Distortion-Decoding-Complexity for Versatile Video Coding *Mingming Zhang, Jialin Li, Jiazhen Wang, Yao Li, Xinmin Feng, Zhuoyuan Li, Li Li, Dong Liu*
2423	11.1	Content-Driven Frame-Level Bit Prediction for Rate Control in Versatile Video Coding *Amritha Premkumar, Prajit T Rajendran, Vignesh V Menon, Christian Herglotz*



Specialized Hardware for Embodied AI Application and Neuromorphic Computing II Session

Session Code:	**C2L-13**	**Date & Time:**	**Wednesday May 27, 2026 (10:30 - 12:00)**
Conference Room:	**5A**	**Chairs:**	**Yueting Li, Bo Li**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1524	15.13	A 442.42 TOPS/W RRAM-Based Digital Computing-in-Memory Accelerator for BF16×1-Bit Vision Transformer *Jingyun Gu, Weiran Chen, Jiaqi Yang, Jingyao Dong, Qilong Chen, Dingbang Liu, Xu Shi, Wei Mao, Jiang Xu, Hao Yu*
2051	15.13	IDEA: A Real-Time Unified Accelerator for Dual-Task Image Restoration: Dehazing and Illumination Enhancement *Gaoxiang Wu, Jingke Wang, Liang Chang, Sichen Liu, Jiahao Zeng, Liang Zhou, Jun Zhou*
1080	15.13	SPICA: Energy-Efficient SRAM-Based Multi-Precision Multi-Mode Compute-in-Memory Accelerator for AI Inference *Xiguang Wu, Pengcheng Yang, Xingyu Zhu, Yuze Li, Yue Ma, Zhou Wang, Jiuren Zhou, Yan Liu, Genquan Han*
2805	15.13	GATPE: A High-Performance Edge-Device GAT Processor with Multi-Layer Data-Variation Mechanism *Zhou Wang, Bin Wang, Haochen Du, Zhou Shu, Jiuren Zhou, Xiguang Wu, Qiankun Li, Yanqing Xu, Hanqi Feng, Xiaonan Tang, Shushan Qiao, Yang Liu, Anil A. Bharath, Emm Mic Drakakis*
2476	15.13	LUT-SNN: Efficient Spiking Neural Networks with Fast Parallel Inference *Mingxin Guo, Qianpeng Li, Jian Cheng, Liang Chen*

Flexible Electronics Session

Session Code:	**C2L-14**	**Date & Time:**	**Wednesday May 27, 2026 (10:30 - 12:00)**
Location:	**5B**	**Chairs:**	**Mayank Kumar Singh, Tong Ge**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2725	18.1	Physics-Guided AI-Assisted Modeling of Flexible Transistors Based on Fully-Additive Printed Electronics Process *Ao Zhang, Tong Ge*
2107	18.1	Resistive Switching of 2D Material Incorporated Polymer Based Self-Healing Flexible Memristor *Parvathy M S, Remya Kunjuveettil Govind, Alex James*
2052	18.1	Comparative Evaluation of Compensation Pixel Circuits Under Bending-Induced Degradation *Shubham Ranjan, Sparsh Kapar*
1910	15.8	A Smart Ring for Long-Term Blood Pressure Monitoring *Jiarong Chen, Min Wang, Bin Liu, Cheng Chen, Guoxing Wang*

RF Switches, Couplers, and Phase Control Session

Session Code:	**C3L-01**	**Date & Time:**	**Wednesday May 27, 2026 (13:30 - 15:00)**
Location:	**3C**	**Chairs:**	**Jusung Kim, Gaetano Palumbo**

Papers are listed in the order they will be presented.

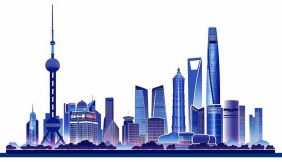
Paper Id	Topic	Title/Author
1281	1.2	A High-Power Absorptive-Type Asymmetric SPDT Switch for Millimeter-Wave Phased-Array Transceiver Front-End *Yi-Fan Tsao, Yi-Hua Chen, Heng-Tung Hsu*
1937	1.2	A 8-40 GHz SPDT Switch with 1.24-dB Insertion Loss and 25.5-dBm IP1dB in CMOS SOI *Zhe Li, Kaixue Ma, Keping Wang*
2399	1.2	Design of Symmetric Transformer-Based Quadrature Couplers *Hanwei Wang, Jiayu You, Ronghua Ni, Xiaohua Yu*
2691	1.2	A 60-GHz Transformer-Based Broadband 3-Way Quadrature-Phase Coupler in 65-nm CMOS *Borun Li, Xin An, Kai Yang, Yunjie Zhao, Tao Zhang, Qijun Lu, Zhangming Zhu*
1333	1.2	A D-Band CMOS Frequency Sextupler with 1.62-dB Conversion Gain and >20-dBc HRR in 65-nm CMOS *Qingfeng Zhang, Hehao Gong, Chenxi Zhao, Kai Kang*

Precision and Low-Noise Amplifiers Session

Session Code:	**C3L-02**	**Date & Time:**	**Wednesday May 27, 2026 (13:30 - 15:00)**
Location:	**3I+3J**	**Chairs:**	**Salvatore Pennisi, Jose Martinez**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1097	1.1	A 3.05 nV/√Hz Bulk-Gate-Driven Inverter-Based Amplifier for High-Temperature Applications *Hendrik Siemssen, Christoph Hillmer, Bernhard Wicht*
1862	1.1	A 0.156 NEF Transimpedance Amplifier with Analog-Domain Multi-Band Fusion Technique for High-Sensitivity and Broadband Hydrophones *Hongye Sheng, Jiao Xia, Yaohui Luan, Xinhang Xu, Zhiyuan Wu, Xili Wang, Yipeng Lu, Linxiao Shen*
2090	1.1	A 6.5nV/√Hz Chopper Stabilized Amplifier with Dead-Time Ripple Compensation (DT-RC) Technique for Precision Data Acquisition *Emmanuel Amankrah, Mohammed Zakariah, Patricia Tutuani, Randall Geiger*
2493	1.1	A Power-Efficient High-Speed Residue Amplifier with Source-Driven Input *Wei Zhang, Xizhu Peng, He Tang*
2780	1.1	Split Reservoir Capacitor Stacking for Correlated-Level-Shifting in Floating Inverter Amplifiers *Ashwinkumar Ramakrishnan Sivakumar, Ankit Sinha, Vivek Kumar Shukla*



Modeling Methods for Nonlinear Circuits and Systems I Session

Session Code:	**C3L-03**	**Date & Time:**	**Wednesday May 27, 2026 (13:30 - 15:00)**
Location:	**3A**	**Chairs:**	**Erivelton Nepomuceno, Yan Liang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1344	9.3	Experimental Lower-Bound Error for Lyapunov Exponent Estimation Using Switch-Controlled Initial Conditions *Thalita Nazare, Murilo Baptista, Erivelton Nepomuceno*
1951	9.6	Piecewise Modeling of RF Power Amplifiers Using Derivative Analysis and K-Means Clusterization *Carolina Pedrosa, Pierre Almairac, Peter Rashev, Dang-Kièn Germain Pham, Jean-Christophe Nanan, Patricia Desgreys*
1802	9.7	Unmanned Aerial Vehicle Tracking Control Under Multiple Safety Constraints via Linearly Combinable Control Barrier Functions *Haoqi Li, Jiangping Hu, Fan Yang, Bijoy K. Ghosh*
1422	9.6	A Unified Queueing-Based Runtime Evaluation Framework with Uncertainty Modeling for Heterogeneous Computing Platforms *Shao Deng, Shanzhu Xiao, Huamin Tao, Jianxiong Zhou, Hai Yi, Xinyi Wang*
1804	9.7	Robust Safe Tracking Control for UAVs with High-Relative-Degree Constraints via Disturbance-Observer-Based Nonlinear CBFs *Fan Yang, Jiangping Hu, Haoqi Li, Bijoy K. Ghosh*

Low-Power Logic, Circuits & Architectures II Session

Session Code:	**C3L-04**	**Date & Time:**	**Wednesday May 27, 2026 (13:30 - 15:00)**
Location:	**3D**	**Chairs:**	**Bruce Sham, Bo Wang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2158	2.2	Energy Efficient Vector Gather Based on Data Serialization and Pulse Selection *Yanan Yang, Chen Zhang, Bingxi Pei, Xia Zhao, Guangda Zhang, Jian Fang, Yande Jiang, Zhiyong Zhong*
2313	2.2	A Scalable Dual-Input/Output Heap-Based Top-K Unit for Vector Search Accelerators *Ji Soo Kim, Hannah Yang, Sujin Kim, Ji-Hoon Kim*
2363	2.2	Reconfigurable SRAM-Cam for Similarity Index Computation in 22-nm FDSOI *Eman Hassan, K.M.Shadid Hassan, Shaymaa Elshahaby, Mahmoud Al-Qutayri, Baker Mohammad*
2636	2.2	A Low Complexity BPF Polar Decoder Design with Sensitivity-Aware LUT Compression Framework *Bozhi Xiu, Yanjing Zhang, Chenggang Yan, Ke Chen, Bi Wu, Weiqiang Liu*
2748	2.2	A Logic-Assisted Hybrid-Mode Ising Machine Based on a 3D Topology for 3D Path Planning *Runhong Tang, Xiangrui Wang, Yuchao Yang, Yuqi Su*

Design and Verification of Digital Integrated Circuits and Systems II Session

Session Code:	**C3L-05**	**Date & Time:**	**Wednesday May 27, 2026 (13:30 - 15:00)**
Location:	**3E**	**Chairs:**	**Chi-Chia Sun, Yun Wu**

Papers are listed in the order they will be presented.

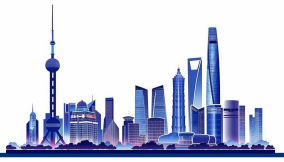
Paper Id	Topic	Title/Author
1726	2.10	DPAM: A Dual-Path Protected Approximate Multiplier for Reliable Neural Network Acceleration *Chao Chen, Yanxi Lin, Haoan Yin, Jilong Zhang, Yan Li, Xiaoyang Zeng*
1877	2.10	Algorithm-Aided Design and Verification for Multiple-Node-Upset-Recovery Latches *Zhiyuan Pei, Jing Li, Haroon Waris, Muhammad Shahzad Younis, Aibin Yan, Jiahui Deng, Yilin Gui, Xiaoqing Wen*
1908	2.10	VeriMaAS: Automated Verilog Code Generation with Multi-Agent Reasoning *Janani Ramamoorthy, Amulya Bhattaram, Ranit Gupta, Diana Marculescu, Dimitrios Stamoulis*
2374	2.5	A High-Precision CORDIC Architecture with Reduced-Convergence Preprocessing and Dynamic Logarithmic Bit-Width Scaling *Zhentao Zheng, Wei Zhang, Jiaqi Ouyang, Qifan Wang, Lei Chen, Fengwei An*
2581	2.5	FPGA-Based High-Parallelism ORB Feature Extraction Accelerator for Visual SLAM *Yang Liu, Qingyu Chen, Yongjiang Xue, Fei Qiao, Qingzeng Song*

Breaking Barriers in Privacy-Preserving Machine Learning: From Algorithms to Accelerators Session

Session Code:	**C3L-06**	**Date & Time:**	**Wednesday May 27, 2026 (13:30 - 15:00)**
Location:	**3B**	**Chairs:**	**Yingjie Lao, Danella Zhao**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1561	15.6	Privacy-Preserving Machine Learning Accelerators: Balancing Efficiency and Security *Bokyung Kim*
1771	15.6	Bridging Trust and Efficiency: TEE-Accelerated Nonlinear Evaluation in Multiparty Computing *Zhuoran Li, Hanieh Totonchi Asl, Ebrahim Nouri, Danella Zhao*
1884	15.6	PEFT: A Near-Memory Processing-Enabled Heterogeneous Accelerator for BatchPBS TFHE *Jiangrui Yu, Yi Chen, Meng Li*
1279	15.6	MOTA: Mapping and Optimization of ASIC-Accelerated TFHE Transciphering *Ran Mao, Zhenyu Guan, Song Bian*
2005	15.6	Time-Area Efficient RNS Base-Conversion Architecture for HPS-BFV Homomorphic Encryption Using Generalized Solinas Primes *Rella Mareta, Ardianto Satriawan, Hanho Lee*



Bridging Algorithms, Circuits, and Systems: Foundations and Applications of Artificial Intelligence Session

Session Code:	**C3L-07**	**Date & Time:**	**Wednesday May 27, 2026 (13:30 - 15:00)**
Location:	**3G**	**Chair:**	**Kai Xu**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1111	15.7	Efficient FPGA Deployment of Power-of-Two Quantized Networks via Dynamic Hierarchical Base-Exponent Offset Encoding *Zongcheng Yue, Zhihang Liu, Sean Longyu Ma, Chiu-Wing Sham*
1846	15.7	WinoMobi: A General-Purpose Winograd IP for Efficient MobileNet Acceleration on Resource-Constrained FPGAs *Yang Zhang, Zongyi Wang, Haotian Chen, Liangzun Fu, Xiwei Huang, Lingling Sun*
1022	15.7	Improving MAC Accuracy of Pre-Aligned Floating-Point CIM Macros for Compound AI with Statistical Group Features *Yunlong Liu, Lichen Feng, Dong Li, Zhangming Zhu*
2010	15.7	A Clock-Independent, Time-Domain Rapid Calibration Method for Memristor-Based Analog Computing AI Processors *Junzhe Chen, Matthew Schormans, Zhiqiang Que, Dinesh Pamunuwa, Jiayang Li*
2004	15.7	A Topology-Aware Reinforcement Learning Framework for 2.4-GHz VSWR-Robust Power Amplifier Matching Network Design *Bingbing Zhao, Hao Tang, Wei-Han Yu, Fabio Passos, Ka-Fai Un, Rui P. Martins, Pui-In Mak*

Energy-Efficient & High-Resolution Data Converters for Next-Generation Biomedical & Neural Interface Session

Session Code:	**C3L-08**	**Date & Time:**	**Wednesday May 27, 2026 (13:30 - 15:00)**
Location:	**5C**	**Chair:**	**Yang Zhao**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2170	15.10	A Sub-μVrms 64-Channel Neural Recording ASIC with Easy-Driven TDM and 16-Bit SAR ADC *Yanxing Suo, Yang Zhao, Yong Lian*
2490	15.10	A 10-MS/s Sub-0.1-mW Power Scalable SAR ADC with 10/12-Bit Reconfigurable Resolution for Portable Ultrasound Systems *Jieming Ni, Yuhao Mao, Wenhao Zhang, Aitong Gong, Xing Wu, Boxiao Liu*
2124	15.10	A 23μW 158.4dB FoM Triple-Slope Current-to-Digital Converter with Digital Thermal Noise Reduction for Electrochemical Current Readout *Minghao Chen, Miao Meng*
1213	15.10	A Reference-Free Neural Network Architecture for ADC Nonlinearity Calibration *Yu Shi, Xuecheng Yang, Yihang Luan, Zuo Zhang, Yilian Zhong, Changde Ding, Zhiliang Hong, Jiawei Xu*
2319	15.10	A 10-Bit Successive Reference Approximation ADC Enabled by Switched-Capacitor Dynamic Reference Generation with Pipelined Pre-Charging and Voltage Ripple Cancellation *Hanlin Xu, Runtao Huo, Yiwen Zhang, Honglan Jiang, Yan Liu, Minmin You, Hui Wang*

Neuromorphic Perception and Control Session

Session Code:	**C3L-09**	**Date & Time:**	**Wednesday May 27, 2026 (13:30 - 15:00)**
Location:	**5F**	**Chairs:**	**Zhuo Zou, Xumeng Zhang**

Papers are listed in the order they will be presented.

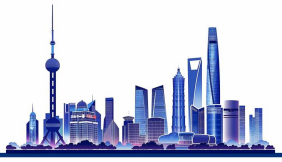
Paper Id	Topic	Title/Author
1227	8.2	FireFly-P: FPGA-Accelerated Spiking Neural Network Plasticity for Robust Adaptive Control *Tenglong Li, Jindong Li, Guobin Shen, Dongcheng Zhao, Qian Zhang, Yi Zeng*
1661	8.2	Neuromorphic Spiking Ring Attractor for Proprioceptive Joint-State Estimation *Federica Ferrari, Flavia Davidhi, Bernard Maacaron, Alberto Motta, Luuk van Keeken, Elisa Donati, Giacomo Indiveri, Chiara De Luca, Chiara Bartolozzi*
2105	8.4	HippNet: A Hippocampus-Inspired Architecture for Spatial Memory and Inference Using CMOS Oscillator Networks *Zongru Li, Wenxiao Cai, Thomas Lee*
2352	8.4	FPGA-Based Spiking Neural Network AutoEncoders for Real-Time Anomaly Detection in LHC Physics *Aqib Javed, Barry Dillon, Jim Harkin*

Image Processing: AI in Circuits and Systems Session

Session Code:	**C3L-10**	**Date & Time:**	**Wednesday May 27, 2026 (13:30 - 15:00)**
Location:	**5D**	**Chairs:**	**Izzet Kale, Yudong Zhang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1441	10.10	WaveMamba: A Vision Backbone Synergizing Feature Extraction and Downsampling *Haitian Yang, Xiangyu Zhang, Yuanmei Zhang, Xin Lou, Wei Zhou*
1505	10.10	A Lightweight Algorithm-Hardware Co-Design for Real-Time Video Frame Interpolation *Jisheng Zhang, Qiwei Dong, Siyu Zhang, Wendong Mao, Zhongfeng Wang*
1834	10.10	CML-UNet: An Adaptive Spatiotemporal Registration Network for Medical Image Sequences *Xinyu Liu, Zhenyu Zhu, Changpeng Shen, Ying Wei*
2439	10.10	Multi-Stage Superpixel-Guided Mamba-Based Network for Change Detection *Jing Liu, Haoyu Yang, Xin Lin, Yuting Su, Peiguang Jing*
2948	10.10	AlignLite: A Lightweight Framework for Weakly Aligned Multimodal Object Detection *Haitian Yang, Xiangyu Zhang, Yuanmei Zhang, Xin Lou, Wei Zhou*



Edge Computing Session

Session Code:	**C3L-11**	**Date & Time:**	**Wednesday May 27, 2026 (13:30 - 15:00)**
Location:	**5H**	**Chair:**	**Xilin Liu**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1527	14.3	A Reconfigurable Multi-Precision MAC with Bin-Based Fp8 Accumulation for Edge AI *Ayush Dixit, Madan Putlekar, Surya Charan Palakurthi*
1758	14.3	MX-SE: Microscaling Data Format with Super Exponent for AI Edge Computing *Tianbo Ming, Yongjian Xu, Bohan Lan, Biwei Liu*
2610	14.6	Mitigating Conductance Drift via In-Situ Calibration for Reliable RRAM-Based CIM Edge Inference *Zhen Kong, Weirong Dong, Junjie He, Zhengke Yang, Jun Lan, Yida Liang, Jiamin Li, Yida Li, Longyang Lin*
1157	14.7	A Discrete-Time Analog Compute Macro for Edge ML with 200 TOPS/W in CMOS 28nm *Farzad Ordubadi, Michael Keyser, Fei Tan, Mahsa Shoaran, Armin Tajalli*
1539	14.7	Hardware-Algorithm Co-Design of a CORDIC-Based Nonlinear Unit for Low-Power Edge RNN Inference *Nazareno Sacchi, Régis Cattenoz, Petar Jokic, Stéphane Emery, Taekwang Jang*

Learning-based Image/Video Coding Session

Session Code:	**C3L-12**	**Date & Time:**	**Wednesday May 27, 2026 (13:30 - 15:00)**
Location:	**5E**	**Chair:**	**Zhu Li**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2024	11.1	On Performance of NNVC Inter-Coding *Xinxin Chen, Nianxiang Fu, Wenzhuo Zhang, Junxi Zhang, Ding Ding, Wenzhuo Ma, Zhenzhong Chen*
2884	11.2	Post-Training Quantization for Overfitted Neural Image Coding *Yile Tu, Heming Sun*
1954	11.2	A Rate-Distortion-Complexity Analysis of Neural Video Codecs *Ricardo de Queiroz, Diogo Garcia, Yi-Hsin Chen, Ruhan Conceição, Wen-Hsiao Peng, Luciano Agostini*
2574	11.3	Training-Free Adaptation from Visible to Thermal Domain for Learned Image Compression *Jiawang Liu, Hualong Yu, Lu Yu*
2632	11.2	Salient-Channel-Guided Knowledge Distillation in Learned Image Compression *Jinhao Wang, Cihan Ruan, Nam Ling, Wei Wang, Wei Jiang*

Analysis and Optimization of Complex Systems and Artificial Intelligence Applications I Session

Session Code:	**C3L-13**	**Date & Time:**	**Wednesday May 27, 2026 (13:30 - 15:00)**
Location:	**5A**	**Chair:**	**Xi Zhang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1648	15.2	AdaCGen: Heterogeneity-Aware Layer Management for Efficient KV Cache Offloading in LLMs *Yujiao Wang, Jiayi Guo, Zongjie Wang, Yujuan Tan*
2216	15.2	VecIntrinBench: Benchmarking Cross-Architecture Intrinsic Code Migration for RISC-V Vector *Liutong Han, Chu Kang, Mingjie Xing, Yanjun Wu*
2764	15.2	TurboRANSAC: A Fully GPU-Accelerated RANSAC Framework for Robust Estimation *Yifan Chen, Feiyang Xin, Zhen Yao, Shuhan Wu, Xin Lou*
2731	15.2	The Similarity Interaction Mechanism Optimizes Multi-Agents with Reactive Strategies *Jiancheng Zhao, Jing Zhang, Biheng Zhou, Yixin Yang, Shaoxuan Xu, Zhihai Rong*

Advanced Circuits and Systems for High-Speed Data Links and Wireless Connectivity Session

Session Code:	**C5L-03**	**Date & Time:**	**Wednesday May 27, 2026 (16:00- 17:30)**
Location:	**3A**	**Chairs:**	**Li Gao, Pei Qin**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1836	15.1	A High Selectivity 28/39GHz Reconfigurable Dual-Band LNA with sub-10 mW for 5G Applications *Yanchen Lin, Li Gao, Xiu Yin Zhang*
2269	15.1	A Broadband Ultra-Compact Series Doherty Power Amplifier Achieving Back-Off Efficiency Enhancement Over 24-to-38GHz in 65nm Bulk CMOS *Hanyu Lu, Pei Qin, Quan Xue, Weijie Chen*
2640	15.1	A 28-Gbps 28-nm CMOS Wireline Receiver Analog Front End with an Adaptive CTLE Enabled by a Hexagonal Mask Eye-Opening Monitor *Yixing Jiang, Runtao Huo, Weihao Jie, Yan Liu, Minmin You, Jingquan Liu, Hui Wang*
2034	15.1	A Single-Ended Tri-Mode PAM2/3/4 Transceiver Front-End Achieving 0.437/0.302/0.314 pJ/Bit Energy Efficiency for D2D Interconnection *Hao Chang, Huajin Sun, Chenxi Han, Zhanming Gao, Yilong Dong, Yuhao Zhang, Lin Wang, Xiaoteng Zhao, Shubin Liu, Zhangming Zhu*
1830	15.1	Resonant Network Optimization and Coupling-Aware Adaptive BPSK Design for High-Speed Inductive Data Links *Yunfang Zhang, Yang Zhao, Yong Lian*

Low-Power Logic, Circuits & Architectures III Session

Session Code:	**C5L-04**	**Date & Time:**	**Wednesday May 27, 2026 (16:00- 17:30))**
Location:	**3D**	**Chairs:**	**Yuan Du, Hongbin Sun**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2761	2.2	EvoGabor: Hierarchical Clustering and Evolutionary Algorithms for Area-Power Efficient Gabor Design *Priyanka Agarwal, Sharan Math, Yash Prasad, Madhav Rao*
2833	2.2	A Low-IF GFSK Demodulator Achieving 0.1% BER Under ±450 kHz Frequency Offset via Dynamic Fractional Delay Calibration *Ruming Guo, Weijia Zeng, Tuo Hu, Meng Liu, Jing Feng, Qiang Li, Hao Min*
2856	2.1	Approximate Reciprocal-Based Divider *Ali Ghaderi, Nima Amirafshar, Hadi Shahriar Shahhoseini, Nima TaheriNejad*
2873	2.1	A Multi-Channel Bioelectric Signal Transmission Device Featuring Low-Power Design *Mingwen Xiao, Xiliang Liu, Minqian Zheng, Zhe Zhao, Milin Zhang*
2877	2.2	An ASIC Emulated Oscillator Ising/Potts Machine Solving Combinatorial Optimization Problems *Yilmaz Ege Gonul, Baris Taskin*

Circuits and Systems for Physiological Sign Detection and Risk Warning in the Elderly Session

Session Code:	**C5L-05**	**Date & Time:**	**Wednesday May 27, 2026 (16:00- 17:30))**
Location:	**3E**	**Chair:**	**Zhao Jian**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2333	15.8	An ISFET Based Multi-Modal Low-Power Chopper-Stabilised Analogue Front-End for Wearable Physiological and Sweat Monitoring *Shuanghua Liu, Haotian Yuan, Junming Zeng, Pantelis Georgiou*
2790	15.8	A Time-Efficient 2D Numerical Compact Model for Dynamic Vascular Monitoring in Functional Near Infrared Spectroscopy Systems *Bangmin Zhu, Xiafan Gu, Wenyao Chen, Jian Zhao, Yibang Chen*
2892	15.8	GenFall: A Configurable Fall Dataset Generated via Text-to-Motion Models for Wearable Fall Detection *Zhipeng Guo, Xiafan Gu, Ting Liu, Eva Guttmann-Flury, Jiajun Yuan*
2889	15.8	Energy-Efficient Fall Detection Using Conditional Dual-Path Spiking Neural Networks with Hierarchical Temporal Dynamics *Xiangting Li, Yangyang Huang, Linxiang Su, Siqiong Yao, Yongfu Li, Jian Zhao*
3000	15.8	A Synchronous EEG-fNIRS BCI: A Proof-of-Concept for Multimodal Avalanche Analysis of Motor Cognition in Older Adults *Eva Guttmann-Flury, Yun-Hsuan Chen, Qiaoyuan Xiang, Hao Zhang, Mohamad Sawan*

Cross-Layer Innovation in Computer-in-Memory Chips Session

Session Code:	C5L-06	Date & Time:	Wednesday May 27, 2026 (16:00- 17:30))
Location:	3B	Chair:	Haozhe Zhu

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1377	15.17	GPA: A General-Purpose In-Memory Computing Accelerator *Xiaoyu Zhang, Zerun Li, Rui Liu, Libo Shen, Boyu Long, Xueqi Li, Yinhe Han, Xiaoming Chen*
2510	15.17	CIM-Pruner: A Dual-Mode Compute-in-Memory Macro for Efficient VLMs with Intra-Chunk Token Pruning and Merging *Zhuojun Han, Siqi He, Chixiao Chen, Haozhe Zhu*
2995	15.17	A BEOL Ferroelectric FET-Based Computing Unit for Digital Computing-in-Memory *Junyu Zhu, Zexue Bian, Weizeng Li, Junzhe Shen, Hanghang Gao, Zhidao Zhou, Zhongze Han, Zhi Li, Hongyang Hu, Qing Luo, Chunmeng Dou*
2996	15.17	A Hybrid RRAM-FeRAM Computing-in-Memory Architecture with Adaptive Quantization Scheme for Edge AI Devices *Honghu Yang, Runru Yu, Tianci Cai, Jianguo Yang*
1659	15.17	An RRAM-Based Multi-Timescale Spiking Processor with Reconfigurable Neurons *Jinhao Liang, Chenyang Li, Fangduo Zhu, Yiwen Zhu, Siyuan Ouyang, Jingsong Zhang, Xumeng Zhang, Qi Liu, Ming Liu*

Application-Specific Computer Arithmetic for Post-Quantum Cryptography & Homomorphic Encryption Access Session

Session Code:	C5L-07	Date & Time:	Wednesday May 27, 2026 (16:00- 17:30))
Location:	3G	Chair:	Amir Sabbagh Molahosseini

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1540	15.3	Efficient On-the-Fly Twiddle Factor Generation for Falcon PQC NTT/INTT *Ghada Alsuhli, Hani Saleh, Mahmoud Al-Qutayri, Baker Mohammad, Thanos Stouraitis*
1750	15.3	A Bitwidth-Flexible Modular Multiplier with Shift-Free Accumulation for Efficient NTT Acceleration in FHE *Zihao Yang, Dian Jiao, Shengyu Fan, Xianglong Deng, Rui Hou, Mingzhe Zhang*
2973	15.3	@NTT: Algorithm-Targeted NTT Hardware Acceleration via Design-Time Constant Optimization *Mohammed Nabeel, Mahmoud Hafez, Michail Maniatakos*
2625	3.8	CEDAR: A Compact and Efficient Decoder Architecture for RS-RM Code in HQC *Yazheng Tu, Tianyou Bao, Jiafeng Xie*
2184	15.13	FeRAM-Based Reconfigurable Strong PUF with Ultra-Low Power and Enhanced Attack Resilience *Xiguang Wu, Yue Ma, Pengcheng Yang, Bo Li, Jiuren Zhou, Wei Mao, Bing Chen, Zhou Wang, Yang Liu, Yan Liu, Genquan Han*

Integrated Circuits and Systems for Intelligent Edge and Biomedical Applications Session

Session Code:	**C5L-08**	**Date & Time:**	**Wednesday May 27, 2026 (16:00- 17:30))**
Location:	**5C**	**Chairs:**	**Hong Zhang, Qinyu Chen**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2248	15.12	CIMS: A CAM-Based In-Memory Sorting Architecture for Efficient Top-K Ranking *Yuhan He, Siheng Lei, Tianxi Hu, Rui Qiao, Li-Rong Zheng, Zhuo Zou*
1808	15.17	An RRAM-Based Neuromorphic Sleep Monitoring System for Energy-Efficient Edge Healthcare Applications *Jingyi Chen, Fangduo Zhu, Zhicheng Li, Zihan Xu, Yiwen Zhu, Jingsong Zhang, Jinhao Liang, Xumeng Zhang, Qi Liu*
1092	15.12	SHAP-AAD: DeepSHAP-Guided Channel Reduction for EEG Auditory Attention Detection *Rayan Salmi, Guorui Lu, Qinyu Chen*
2685	15.12	Hardware-Efficient POSIT Based SVM Inference Engine for Intelligent Biomedical Systems *Arun M, Vaishnavi Sharma, Madhav Rao*

Quantization, Approximation, and Compression for ML Hardware II Session

Session Code:	**C5L-09**	**Date & Time:**	**Wednesday May 27, 2026 (16:00- 17:30))**
Location:	**5F**	**Chair:**	**Joseph Schmitz**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1276	14.3	A Graph-Based Methodology for Dynamic KV-Cache Compression in Transformer Inference *Neermita Indranil Bhattacharya, Shyam Sathvik, Abhishek Yadav, Ayush Dixit, Binod Kumar*
2251	14.1	A FeFET-Based Approximate DCIM Integrating Multiplication and or Addition In-Bitcell *Jangseok Yu, Taehwan Kim, Seunghwa Hyun, Jongsun Park*
2613	14.3	HHGC: High-Throughput High-Accuracy Gradient Data Compression *Yupeng Gui, Xinglin Wei, Yanwu Liu, Leilei Huang, Xiao Yan, Yibo Fan*
1773	14.2	ViMA: A Decoupled FPGA Accelerator for Vision Mamba with Resource-Space Exploration *Yu Qi, Jin Tang, Tao Zhang, Zhicheng Zhang, Jianqin Yin*
2148	14.6	An FPGA-Based Design of Reliable Quantized AdderNet Under Fault Injection *Rong Tian, Huiyang Jin, Yanmao Qi, Zhen Gao, Biao Sun*

Compressive Sensing and Sparse Signal Processing Session

Session Code:	**C5L-10**	**Date & Time:**	**Wednesday May 27, 2026 (16:00- 17:30))**
Location:	**5D**	**Chairs:**	**Deruo Cheng, Wing-Kuen Ling**

Papers are listed in the order they will be presented.

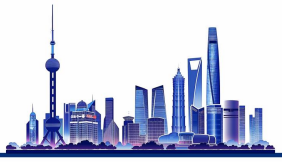
Paper Id	Topic	Title/Author
1872	10.4	Edge-RamanSBL-Net: Compressed Sensing-Based Real-Time Directional Raman Qualitative Unmixing via Network Unfolding and One-Shot Training *Jinglei Zhai, Bowen Mao, Pei Liang, Biao Sun*
1899	10.4	Accelerating Audio-Driven 3D Facial Animation Training with a Compressive Sensing Framework *Hongzhen Chen, Lei Sun, Jiuwen Cao, Zhiping Lin*
2149	10.4	Compressive Light-Field Image Coding with Spatial-Angular Measurement Prediction *Ayumu Seki, Akihiro Sakurai, Jinjia Zhou*
2288	10.4	A Novel Frequency Detection Method Based on Aliasing Sampling System *Jiahui Ding, Yi Zhang, Yijiu Zhao, Naixin Zhou*
1815	10.4	FPGA-Accelerated Real-Time Image Reconstruction for CMOS Electrochemical Sensing Arrays *Tom Zhou, Shuanghua Liu, Pantelis Georgiou*

Cross-Layer Optimization for Machine Learning Session

Session Code:	**C5L-11**	**Date & Time:**	**Wednesday May 27, 2026 (16:00- 17:30))**
Location:	**5H**	**Chair:**	**Ibrahim Elfadel**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1487	14.5	ICDL: Inverse Compensation Direct Learning with Model-Accelerator Co-Optimization Enabling Real-Time Inference in Precision Motion Control *Manni Li, Longbin Jiang, Zixu Li, Jiayu Yang, Zijian Huang, Wending Zhao, Yinyin Lin, Xiaofeng Yang*
1586	14.7	HiMARS: High-Performance Inference for Multi-Modal/Model AI Assistant via Runtime Scheduling *Maoliang Li, Jiayu Chen, Zihao Zheng, Chenchen Liu, Weisheng Zhao, Xiang Chen*
1820	14.5	Efficient LoRA-Based Weight Update Write-Back in 3D NAND Flash for Large Language Models *Dongxue Zhao, Tianyang Luo, Ling Liang, Zongwei Wang, Yimao Cai*
2511	14.5	A Reconfigurable Audio Analog Front-End with Hardware-Aware Transfer Learning for Task-Adaptive Keyword Spotting *Jinhai Hu, Zhongyi Zhang, Wang Ling Goh, Yuan Gao*
2756	14.1	Cross-Layer Evaluation for On-Chip Training of BEOL FeTFT-Based CIM M3D Accelerator *Wei Zhang, Jianze Wang, Yimin Wang, Xuanyao Fong*



Volumetric video coding and communication Session

Session Code:	C5L-12	Date & Time:	Wednesday May 27, 2026 (16:00- 17:30))
Location:	5E	Chair:	Lu Yu

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2585	11.9	Volumetric Video on Demand System Based on Scalable Spacetime Gaussian Splatting *Yuhang Li, Junyi Lu, Jun Xu, Bingcong Lu, Rong Xie, Li Song*
2292	11.9	Dual-Hilbert Scan for Efficient Video-Based Gaussian Splatting Compression *Zhiwei Zhu, Yiyi Liao, Lu Yu*
1043	11.8	GFix: Perceptually Enhanced Gaussian Splatting Video Compression *Siyue Teng, Ge Gao, Duolikun Danier, Yuxuan Jiang, Fan Zhang, Nantheera Anantrasirichai, Thomas Davis, Zoe Liu, David Bull*
2314	11.6	SENTRY-VQA: A Region-Aware Framework for Surveillance Video Quality Assessment *Min Li, Qi Zheng, Chenlong He, Jiaming Liu, Leilei Huang, Minge Jing, Xiao Yan, Yibo Fan*
1806	11.4	Diff-Band:Bandwidth Estimation in RTC via Diffusion-Based Offline Reinforcement Learning *Bingcong Lu, Jun Xu, Zhengxue Cheng, Li Song, Bingnan Duan, Jintao Fang*

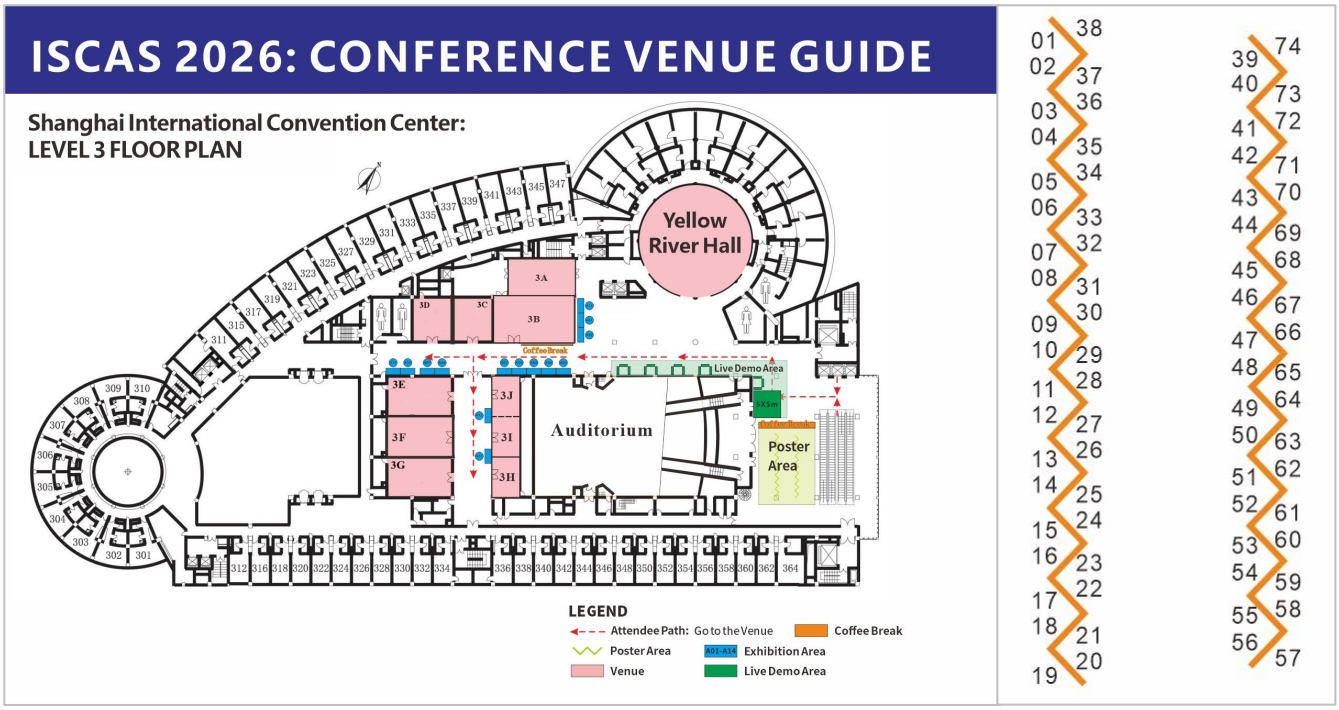
Analysis and Optimization of Complex Systems and Artificial Intelligence Applications II Session

Session Code:	C5L-13	Date & Time:	Wednesday May 27, 2026 (16:00- 17:30))
Location:	5A	Chair:	Xi Zhang

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1889	15.2	SegSEM: Enabling and Enhancing SAM2 for SEM Contour Extraction *Da Chen, Guangyu Hu, Kaihong Xu, Kaichao Liang, Songjiang Li, Wei Yang, Xiangyu Wen, Mingxuan Yuan*
1785	15.2	Multi-Region Thermal–Renewable Coordinated Dispatch Considering Chance-Constrained Reserve and Supply Security *Zhi Cao, Zi'An Li, Liang Wang, Xi Zhang, Wenshuang Liu, Yifei Li, Zhengran Wu*
2115	15.2	Knowledge Distillation in the QAOA Setting for Advantage on Quantum Hardware *Simone Piperno, David Windridge, Giacomo Vittori, Antonello Rosato, Massimo Panella*
2355	15.2	An Explainable Multi-Modal Deep Learning–Enhanced Framework for Automated Depression Detection *Lingfeng Ma, Shengming Zhao, Yuqi Wu, Jie Chen*
2994	15.17	HOPESim: A Lightweight and Modern C++ Based Accelerator Simulation Approach *Xueqi Li, Ruihao Gao, Xiaoyu Zhang, Xiaoming Chen, Shunchen Shi, Fan Yang, Ninghui Sun*

Poster Session Assignments & Guidelines



1.Important Notes

- **Identification:** The 4-digit numbers in the table refer to your Paper ID.
- **Poster Board:** Please locate your assigned Poster Board Number (1–80) in the Poster Hall according to the layout map.
- **Removal:** Posters remaining after the 30 minute teardown window will be cleared by the PCO staff.

2.Daily Schedule (May 25 – 27)

To ensure a smooth transition between sessions, please strictly follow the schedule below:

Morning Session: 10:00 – 12:00

- **Set-up: 09:30 – 10:00**
- **Presentation: 10:00 – 12:00**
- **Teardown: 12:00 – 12:30**

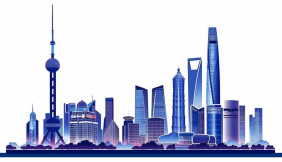
Afternoon Session: 14:30 – 16:30

- **Set-up: 14:00 – 14:30**
- **Presentation: 14:30 – 16:30**
- **Teardown: 16:30 – 17:00**

3.Location: SHICC Lobby, Level 3

4.Poster Specifications

- **Maximum Size: 90cm (Width) x 120cm (Height).**
- **Orientation: Portrait (Vertical) orientation only.**



5.Assignment Table

	25-May		26-May		27-May	
Poster Board	**10:00 – 12:00**	**14:30 – 16:30**	**10:00 – 12:00**	**14:30 – 16:30**	**10:00 – 12:00**	**14:30 – 16:30**
1	1397	2033	1714	1621	1181	1220
2	1993	2126	2028	2075	2059	1312
3	2137	2404	2056	2116	2227	1689
4	2631	2642	2063	2323	2572	2917
5	2967	2734	2141	1474	1318	1257
6	1030	2139	2246	1704	2120	1400
7	1240	2544	2415	2095	2370	1529
8	1347	2714	2813	2470	1429	2540
9	2191	2716	2711	2635	1464	2649
10	1125	2931	2910	1239	1016	1473
11	2062	1024	1288	1247	1565	2488
12	2353	1045	1606	1311	1868	1584
13	1593	1087	1807	2147	1967	2000
14	1766	1335	2218	2617	2763	1301
15	2243	1533	1103	1175	1514	1591
16	2416	1922	1384	1388	1712	1744
17	2645	1956	1572	1401	2209	1898
18	1285	2477	2193	1499	2233	2465
19	2019	2746	1226	2206	1811	2578
20	2167	2773	1255	2590	2247	1373
21	2614	1038	2541	2677	2568	1851
22	1395	1156	1405	2776	2651	2254
23	1569	1955	1978	2863	2914	2758
24	1886	2491	1065	2883	1291	2778
25	2396	2526	1121	1141	2844	2907
26	2461	1117	1538	1262	2943	2076
27	2485	1207	1813	1506	1819	2317
28	2652	1631	2947	1597	2194	2950
29	2684	1893	2633	2391	2362	2881
30	2707	2729	2935	2475	2623	1535
31	1136	1195	1237	1943	2845	2533
32	1582	1442	1740	1093	1376	2626
33	1728	1697	2199	1314	1512	2819
34	2162	2097	2507	1681	1613	1928
35	2886	2180	1776	2087	2144	1416

36	2451	2344	1995	2294	2607	1081
37	1177	2402	1286	2296	1349	1252
38	2523	2666	1517	1973	1453	1852
39	2598	2730	1864	2518	1542	2838
40	1137	2401	2271	1354	1604	1039
41	1163	1054	1077	1595	1755	1292
42	1724	1122	1677	1805	2035	1664
43	1607	1662	1900	2186	2045	1752
44	1619	2185	2205	2264	2252	1507
45	1623	1317	2300	2295	2273	2434
46	1828	1458	2701	2413	2600	2534
47	2156	1596	2817	2460	1536	2551
48	2471	2286	1223	2503	1767	1684
49	1508	2916	2438	2719	1883	1892
50	1066	1009	2799	2990	2044	2663
51	2153	1679	2911	1962	1598	2801
52	2381	2067	1427	2679	1212	2998
53	1879	2068		1444	1645	1855
54	1176	2432		2187	1692	2811
55	2977	1004		2620	1919	1185
56		1008		2628	2182	1774
57		1287		1396	2505	2603
58		1323		2008	2565	1778
59		1451		2027	2591	2298
60		1106		2421	2848	2839
61		1489		1261	1109	1580
62		1737		2303	1234	2757
63		2312		2305	1406	1316
64		2446		2888	2525	1402
65		1695		1644	2928	1765
66		1711		1730	1154	2239
67		2192		1965	1699	2885
68		2890			1777	
69		1145			1904	
70		1478			2332	
71		1703				
72		2032				
73		1660				

Poster Session Schedule- Detailed Agenda

RF and mm-Wave Front-End Circuits Session

Session Code:	**A1P-20**	**Date & Time:**	**Monday May 25, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Cindy Tam, Liangjian Lyu**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1397	1.2	A CMOS E-Band Noise-Canceling Low Noise Amplifier with 4.5 dB Noise Figure *Lingtao Jiang, Shangyao Huang, Xianfeng Que, Bing Cai, Yanjie Wang*
1993	1.2	Design of a / -Band Mode-Switching Reconfigurable Low-Noise Amplifier in 110-nm CMOS Technology *Hongjie Zeng, Xiuping Li, Yubing Li, Tao Tan*
2137	1.2	A Compact Broadband Power Amplifier with High Efficiency and <1% Power-Added Efficiency Variation Over 24–36 GHz *Yunhan Qian, Yu Tao, Chunqi Shi, Leilei Huang, Jinghong Chen, Runxi Zhang*
2631	1.2	High-Selectivity RF On-Chip Dual-Passband Filter with Multiple Stopband Transmission Zeros Using Through-Glass-Via Technology *Wei Wei, Li Yang, Jin-Xu Xu, Xi Zhu, Roberto Gómez-García, Xiu Yin Zhang*
2967	1.2	Indirect Multi-Domain Characterization of 25 GHz 5G Amplifiers Using a Low-Cost SDR and IF-Loopback Testbed *Rodrigo Apaza Huanca, Renan Garcia Escarzo, Juan Carlos Paredes Condori, Esteban Gironda Lagrava, Florencia Tabata Pi...*

RF and mm-Wave Transmitter and Frequency Generation Session

Session Code:	**A1P-21**	**Date & Time:**	**Monday May 25, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Ankesh Jain, Degang Chen**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1030	1.2	A 41-62.4 GHz CMOS Frequency Doubler with Peak 30.79% Drain and 13.7% Total Efficiency *Harikrishna Kambham, Praful Mankar*
1240	1.2	A New Triple-Quadrature Image-Rejection Architecture for mm-Wave Applications *Kejie Hu, Xu Wang, Yue Hu, Zhipeng Wang, Enlin Wang, Weiwei Zhou, Yongrong Shi, Kaixue Ma*
1347	1.2	A Novel Segmentation Approach Based on Analog LSB for High-Resolution mmWave Digital TXs *Niek Kesteloo, Lennart Detje, Vojkan Vidojkovic, Dusan Milosevic, Georgi Radulov*
2191	1.2	A Low-Power 4x Multiplier Based on Current-Reuse Complementary Push-Push Doublers *Manfredi Caruso, Andrea Ballo, Minoo Eghtesadi, Salvatore Pennisi, Gianluca Giustolisi, Egidio Ragonese*

Low-Noise Analog Amplifiers and Filters Session

Session Code:	**A1P-22**	**Date & Time:**	**Monday May 25, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Vanessa Chen, Randall Geiger**

Papers are listed in the order they will be presented.

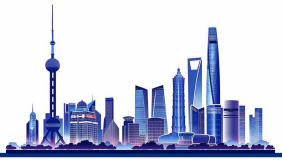
Paper Id	Topic	Title/Author
1125	1.1	Power-Efficient Gm–C Band-Pass Filter for Bio-Signal Acquisition *Ahmed Reda Mohamed*
2062	1.1	A 241MHz/mA Low Power, Low Noise Capacitively Coupled Chopper Amplifier with Integrated Feedforward Passive Ripple Reduction *Mohammed Zakariah, Emmanuel Amankrah, Patricia Tutuani, Randall Geiger*
2353	1.1	Zero-Crossing Aligned and Self-Fill-In Chopping for IMD-Free Chopper Amplifiers *Xinyu Xie, Zeyu Cai*

AI and Automation-Assisted Analog/RF Design Session

Session Code:	**A1P-23**	**Date & Time:**	**Monday May 25, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Keren Zhu, Hyeon Kim**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1593	1.8	HOLMES: Hierarchical Optimization with Polygonal Modeling for Large-Scale AMS Placement *Guanhua Chen, Yujie Yan, Jiahua Liu, Zecheng Xu, Linxi Qiu, Yumao Wu, Zhiang Wang, Changhao Yan, Zhaori Bi, Keren Zhu*
1766	1.8	Design Automation and Optimization of Double Balanced Gilbert-Cell I/Q Mixers *Lakshmi Sai Krishna Yarru, S Ramprasath, Subhanshu Gupta, Sankaran Aniruddhan*
2243	1.1	Topology-Aware GNN Embedding with Domain Priors and Graph Policy Regularization for Balanced Multi-Objective Analog IC Design *Lintao Tang, Jintao Li, Zhenxin Chen, Kun Huang, Yongfu Li, Yanhan Zeng*
2416	1.8	EM-Aware Physical Synthesis: Neural Inductor Modeling and Intelligent Placement & Routing for RF Circuits *Yilun Huang, Asal Mehradfar, Salman Avestimehr, Hamidreza Aghasi*
2645	1.6	Cross-Resolution Transfer Learning in Pixelated RF Filter Inverse Design *Jingyun Bi, Xiaoyang Yu, Xiaofei Hu, Xinyu Zhou*



Wireline Communications II Session

Session Code:	**A1P-24**	**Date & Time:**	**Monday May 25, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Yuan Du**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1285	3.1	A 17.28-Gb/s Transceiver with Hybrid Phase-Interpolated Clock and Data Recovery in 40-nm CMOS *Shuo Han, Sheng-You Liu, Kai-Hung Chou, Min-Shu Shih, Ping-Heng Wu, Ching-Yuan Yang*
2019	3.1	A 32-Gb/s Adaptive DFE with Dynamic Step SSLMS Achieving 0.9 μs Convergence *Liu Wang, Chang Liu, Zhiwei Wei, Xiao Ma, Bo Li*
2167	3.1	A Crossed Bond-Wire Structure for High-Speed Differential Interconnects Achieving 27% Reduction in Insertion Loss at 56 GHz *Hangyu He, Yang Shen, Yuhang Zhang, Xiaojin Li, Yanling Shi, Bingyi Ye, Yabin Sun*
2614	3.1	A 30Gb/s/pin PAM3 Single-Ended Transceiver with Crosstalk-Cancelling Coding for Memory Interfaces *Qian Liu, Yiheng Hui, Yiwei Xu, Zhiqiang Zhang, Li Du, Yuan Du*

Wireless Communications III Session

Session Code:	**A1P-25**	**Date & Time:**	**Monday May 25, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Kyungki Kim**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1395	3.2	On the Purpose of Harmonic Suppression: A Two-Stage Approach Enabling ACPR Enhancement for VMbPWM-Based All-Digital Transmitter *Yujie Xian, Jiyi Liu, Kaijiang Li, Kai Gao, Shang Ma*
1569	3.2	Neural Network-Based Contiguous Carrier Aggregation Digital Predistortion Design for Sub-THz Power Amplifier in Baseband Transmitter *Cheng-Hsuan Lai, Chung-Lun Tu, Yi-Shan Huang, Shyh-Jye Jou*
1886	3.2	A Highly Efficient Reconfigurable All-Digital DLL-Based RF Transmitter Using Phase Interpolation in 22nm FDSOI *Philipp Nickel, Deguang Sun, Robin Staub, Jendrik Kellermann, Andreas Wentzel, Friedel Gerfers*
2396	3.2	Analytical Origin and Mitigation of Third-Order Tones in 4-Phase BLE Backscatter *Jeong Gyu Cho, Min-Jun Suh, Ju-Won Oh, Yeon-Jae Jung, Ealwan Lee, Sungjin Kim, Kang-Yoon Lee*

Image Processing Session

Session Code:	**A1P-26**	**Date & Time:**	**Monday May 25, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Wing-Kuen Ling, Deruo Cheng**

Papers are listed in the order they will be presented.

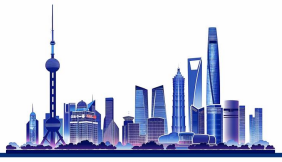
Paper Id	Topic	Title/Author
2461	10.10	SEP-YOLO: Fourier-Domain Feature Representation for Transparent Object Instance Segmentation *Fengming Zhang, Tao Yan, Jianchao Huang*
2485	10.10	SEE: An Efficient Feature-Based Framework for Performance Prediction in Semantic Segmentation *Felix Deichsel, Yongxu Ren, Philipp Beckerle, Jürgen Seiler, Ándre Kaup*
2652	10.10	FPGA-Based Hardware Optimization for Low-Power High-Speed NLM Algorithms *Ruihang Guo, Tianyu Yan, Jiongyao Ye, Lianbo Wu*
2684	10.10	MK-Net: A Multi-Scale Semantic Propagation and Base-Channel Distillation Network for Multi-Class Kidney Ultrasound Segmentation *Boyuan Chen, Chengjie Liu, Wenbo Qi, Shing Chow Chan*
2707	10.10	An Efficient Low-Light Object Detection Framework Based on Task-Driven Distillation *Haoyan Li, Wei Zhou, Kangjie Long, Cong Pang, Xiangyu Zhang, Xin Lou*

Other Areas in Digital Signal Processing Session

Session Code:	**A1P-27**	**Date & Time:**	**Monday May 25, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Cindy Tam**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1136	10.12	Multi-Source Localization in High-Noise Mixed Fields: A Logarithmic Spacing Multi-Concentric Circular Array and Conical Gridding Method *Chiang Liang Kok, Yuwei Dai, Howard Tang, Fanyi Meng, Tee Hui Teo*
1582	10.12	Near-Field Radar Imaging Motion Compensation Solution Based on STFT and PGA *Yang Zhao, Tianxing Lu, Yingjian Hao, Jingqian Wang, Leilei Huang, Chunqi Shi, Jinghong Chen, Runxi Zhang*
1728	10.12	Node-Edge-Variant Distributed Graph Filter Design with Edge Sparsity *Rui Yang, Aimin Jiang, Yibin Tang, Min Li, Hon Keung Kwan*
2162	10.12	An Automated Framework for Optimal Selection of Approximate Computing Units for Low-Complexity Trigonometric Transforms on FPGAs *Pathmapirian Nanthakumar, Chamith Wijenayake, Chamira Edussooriya, Arjuna Madanayake*
2886	10.12	Low-Complexity Multi-Beamforming with Configurable Beam Profiles via Approximate-DSFT *Pathmapirian Nanthakumar, Chamith Wijenayake, Chamira Edussooriya, Arjuna Madanayake*



Circuits, Systems and Architectures for Machine Learning III Session

Session Code:	**A1P-28**	**Date & Time:**	**Monday May 25, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Ljiljana Trajkovic**

Papers are listed in the order they will be presented.

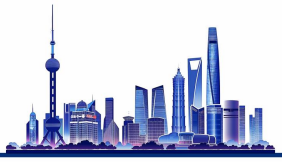
Paper Id	Topic	Title/Author
2451	14.1	LOKI: An LLM Accelerator with Optimized KV Cache and In-Memory Computing Cores *Avadh Rajesh Harkishanka, Abhishek Tyagi, Xuanyao Fong*
1177	14.2	PRIMAL: Processing-in-Memory Based Low-Rank Adaptation for LLM Inference Accelerator *Yue Jiet Chong, Yimin Wang, Zhen Wu, Xuanyao Fong*
2523	14.2	STEAM-SSM: A Streaming-Tiled Efficient Accelerator for Mamba-2 SSM on FPGA *Sehoon Chon, Xuan Truong Nguyen, Minh Nguyen-Duc, Hyuk-Jae Lee*
2598	14.2	VitaLLM: A Versatile and Tiny Accelerator for Mixed-Precision LLM Inference on Edge Devices *Zi-Wei Lin, Tian-Sheuan Chang*
1137	14.7	Reliability and Optimization for Neural Network Accelerators Using Value-Aware Error-Marking Pattern with Sequential Access Error Correction *Jun-Shen Wu, Ren-Shuo Liu*
1163	14.2	A Lightweight RISC-V Multiply-Accumulate Extension with Data Preloading Scheme *Wei-Ting Chen, Meng-Hsueh Lee, Tsung-Te Liu*
1724	14.2	FlexEdge: A Hardware-Software Co-Design for Flexible Edge Transformer Inference *Jiewen Zheng, Zifeng Zhao, Qi Wu, Gengsheng Chen, Wenbo Yin*
1607	14.1	UMDAM: A Unified Data Layout and DRAM Address Mapping for Heterogeneous NPU-PIM *Hai Huang, Xuhong Qiang, Weisheng Zhao, Chenchen Liu*
1619	14.7	InfiNAS: Architecture Search of Infinite-Dimensional Neural Networks *Jiayu Chen, Maoliang Li, Zihao Zheng, Chenchen Liu, Weisheng Zhao, Xiang Chen*
1623	14.1	CxlRatioOpt : A Predictive Optimizer for Performance Trade-Offs in CXL-Tiered Memory *Peng He, Hao Fu, Yue Ma, Bowen Wang, Haiyuan Wan, Zhirun Yue, Sheng Zhang, Fangming Liu*

Media Coding and Representation Session

Session Code:	**A1P-29**	**Date & Time:**	**Monday May 25, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Xin Jin**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1828	11.1	Cross-Platform Low Operation Point In-Loop Filter for VVC Using Integer Operations *Jiang Han, Cheolkon Jung, Qipu Qin*
2156	11.1	Learning-Enhanced Video Compression with Capability Beyond VVC *Wenzhuo Zhang, Luyi Qin, Xinxin Chen, Nianxiang Fu, Haodong Qu, Wenzhuo Ma, Junxi Zhang, Zhenzhong Chen*
2471	11.1	Multiple Candidates Derivation of Dominant Intra Prediction Mode in Beyond VVC *Lu Wang, Junyan Huo, Yanzhuo Ma, Wei Zhang, Fuzheng Yang, Jiarun Song*
1508	11.14	An Efficient Hardware Accelerator for JPEG-AI Image Compression on FPGA *Weize Ma, Sen Gao, Siyuan Leng, Tong Chen, Ming Lu, Zhan Ma, Jun Lin*
1066	11.2	LMM-VSC: Ultra-Low Bitrate Video Compression with Semantic Understanding *Chaolei Liu, Li Song, Chuqin Zhou, Guo Lu*
2153	11.2	FNeRV: Frequency-Aware Neural Video Representations with Dynamic Spatial Guidance *Ziwen Xiong, Yiheng Jiang, Li Li, Dong Liu*
2381	11.2	Learning-Based CU Splitting in VVC: A ConvNeXt Approach for Intra-Mode Acceleration *Md. Zahirul Islam, Asifur Rahman Rahat, Noman Amin, S. M. Faisal, Manoranjan Paul, Zhenni Pan*
1879	11.9	Res-P4DGS:Enhancing 4D Gaussian Splatting Compression with Scene-Depth Prior *Xinliang Gong, Hanxin Zhu, Henan Wang, Xin Li, Zhibo Chen*
1176	11.2	SCONE: A Practical, Constraint-Aware Plug-In for Latent Encoding in Learned DNA Storage *Cihan Ruan, Lebin Zhou, Rongduo Han, Linyi Han, Bingqing Zhao, Chenchen Zhu, Wei Jiang, Wei Wang, Nam Ling*
2977	11.15	Revisiting MLLM Token Technology Through the Lens of Classical Visual Coding *Jinming Liu, Junyan Lin, Yuntao Wei, Kele Shao, Keda Tao, Jianguo Huang, Xudong Yang, Zhibo Chen, Huan Wang, Xin Jin*



Incremental and Delta-Sigma ADCs Session

Session Code:	**A3P-17**	**Date & Time:**	**Monday May 25, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Tong Ge, Raafat Labadibi**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2033	1.3	A 25kHz-BW 115-dB SNDR Zoom Incremental ADC with Two-Step Extended-Counting Technique for Audio Applications *Zhenghang Gao, Shiwei Wang, Mingyi Chen*
2126	1.3	A Hybrid FIR-IIR MASH DTDSM with Optimized Self-Coupling Filter for Robust Low-Amplitude Stability *Chenwang Mo, Jiarun Yuan, Yang Zhao, Yong Lian*
2404	1.3	FIR Feedback in Incremental ΔΣ Modulators with Feedback-Assisted Input-Stage Linearization *Nicolas Graber, Paul Kaesser, Dominik Fritschi, Maurits Ortmanns*
2642	1.3	A MASH Two-Phase Incremental ADC with High Tolerance to QN Leakage *Qingxun Wang, Yuhan Pan, Rui Feng, Yinglong Ding, Liang Qi*
2734	1.3	A Low-Distortion Feedforward Delta-Sigma ADC with Nested Summation Quantizer *Che Qin, Zhengzhe Jia, Xinyu Xie, Zeyu Cai*

CT and DT-CT Delta-Sigma Modulators Session

Session Code:	**A3P-18**	**Date & Time:**	**Monday May 25, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Sohmyung Ha**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2139	1.3	A Highly Linear 5-Level SCDAC with Simple Control Logic for Wideband CTDSMs *Tong Lu, Jiarui Dong, Xian Tang*
2544	1.3	An Intrinsically Linear 9-Level Current-Steering DAC for Continuous-Time Delta-Sigma ADCs *Kaixin Tang, Jesko Flemming, Bernhard Wicht, Pascal Witte*
2714	1.3	A Multi-Rate 2-2 DT-CT MASH DSM Using an Embedded LPF for Easy-Driving *Qingxun Wang, Ziqiang Cai, Rui Feng, Yinglong Ding, Liang Qi*
2716	1.3	On the Degradation of Alias Rejection in Continuous-Time Incremental ΔΣ Modulators *Sayan Banerjee, Ankesh Jain*
2931	1.3	Iterative Time-Constant Tuning for Finite-GBW Compensation in Continuous-Time Delta–Sigma Modulators *Jianhao Yuan, Zhuojian Yao, Fei Chen, Baoyong Chi*

PLLs & DLLs Session

Session Code:	**A3P-19**	**Date & Time:**	**Monday May 25, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Arindam Sanyal, Hongzhi Liang**

Papers are listed in the order they will be presented.

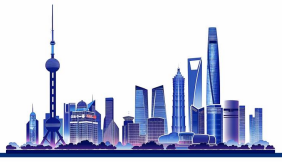
Paper Id	Topic	Title/Author
1024	1.8	Sub-Threshold DLL with Built-in Linearization and Time-Mode Proportional-Integral Locking *Fei Yuan, Wenhao Wu, Yushi Zhou*
1045	1.7	Phase Errors in Sub-Threshold Delay-Locked Loop *Fei Yuan*
1087	1.7	A Wideband PLL Based on a Wide-Tuning-Range Dual-Mode VCO and a High-Speed TSPC Prescaler *Jiawei Shi, Zhiming Chen, Qiaonan Wang, Zicheng Liu*
1335	1.7	A Hybrid PLL Architecture Improving Two-Point Modulation Robustness *Guillaume Melas, Helene Esch, Philippe Level, Jean-Loup Margerin, Yann Deval*
1533	1.7	A Background Calibration Technique in Rotary Travelling Wave Oscillator Based All-Digital PLL *Xing Zhou, Ralph Mason, Rony Amaya*

Oscillators and Clock Generation Session

Session Code:	**A3P-20**	**Date & Time:**	**Monday May 25, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Shahriar Mirabbasi, Robert Sobot**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1922	1.7	Exploring the Phase Noise Reduction Limits of Stacked Ring Oscillators *Gonçalo Rodrigues, Jorge Fernandes*
1956	1.7	An Ultra-Low Power Relaxation Oscillator for IoT Power Management Applications *Abdul Rehman, Yasser Rezaeiyan, Milad Zamani, Farshad Moradi*
2477	1.7	A 70mV Direct Non-Overlapping Clock Generation Using Coupled Ring Oscillator with Stacked-Inverters *Ahmad Almonaier, Sanket Hanamashetti, Soumya Bose*
2746	1.7	A 445pW, 28Hz Gate-Leakage Based Relaxation Oscillator *Dheeraj Gandepalli, Yuvraj Sinh Rathore, Abhishek Pullela, Zia Abbas*
2773	1.7	Design and Analysis of Class-F23 LC-VCO with Wideband Common-Mode and Differential-Mode Impedance Control for Low Phase Noise in 65-nm CMOS *Adarsh Yadav, Saurabh Zope, Abhishek Srivastava*



Hardware Security for Internet-of-Things, Cyber-Physical Systems II Session

Session Code:	**A3P-21**	**Date & Time:**	**Monday May 25, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Wendong Mao**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1038	2.6	A Novel CRP-Space-Extended RO-PUF Based on LFSR and FNV-1a Implemented in 90nm CMOS for IoT Security *Yu-Wei Lee, Yi-Hsiang Tseng, Chi-Chia Sun*
1156	2.6	DeepRevelio: Multivariate Time Series Detection for Stealthy IoT Malware via Variable-Length Entropy Analysis *Zhuoran Li, Danella Zhao*
1955	2.6	Design of a PUF in 600-nm IGZO-TFT Flex-ICs for Secure IoT Applications *Tiago Martins, Joao Cabacinho, Joao Casaleiro, Domenico Rosis, Raffaele Rose, Emanuel Carlos, Pedro Barquinha, Luís Bica Oliveira*
2491	2.6	Efficient and Agile ECC Acceleration: A Hardware/Software Co-Design with Automated Compilation *Yicheng Huang, Xueyan Wang*
2526	2.6	QT-PUF: Quantum Tunneling Leakage Based PUF for Implantable IoMT Devices *Yueqi Ma, Vivek Mohan, Chip Hong Chang, Emm Mic Drakakis*

Programmable, Reconfigurable & Array Architectures II Session

Session Code:	**A3P-22**	**Date & Time:**	**Monday May 25, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Hongbin Sun**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1117	2.5	Top-V: A Flexible and Programmable Top-K Acceleration Framework Based on the RISC-V ISA *Qixiang Chen, Chuanning Wang, Zhongfeng Wang, Jun Lin*
1207	2.5	ARIC: A Lightweight Reconfigurable Active Interposer with Cpu-Free Configuration *Jiashuai Zhang, Xiao Yang, Xici Huang, Chunhua Zheng, Liuqing Yang, Huiyun Li*
1631	2.5	FPGA-Based Dense-Sparse Adaptive Simulated Bifurcation Ising Machine for MAX-CUT Problems *Yihang Peng, Chengjie Wang, Yudi Zhao, Shisheng Xiong*
1893	2.5	FPGA-Accelerated Feature Extraction for an AI-Based Automatic Modulation Classification System *Felipe Ferreira Nascimento, Gracieth Batista, Bruno Sanches, Osamu Saotome*
2729	2.5	MoSim: A Modular Simulation Framework for FPGA-Based Systolic CNN Accelerators *Jin Yuan, Zuwen Ou, Guangjin Li, Ahmed Kamaleldin, Diana Göhringer*

Electronic Design Automation and Physical Design IV Session

Session Code:	**A3P-23**	**Date & Time:**	**Monday May 25, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Tian-Sheuan Chang, Meiqi Wang**

Papers are listed in the order they will be presented.

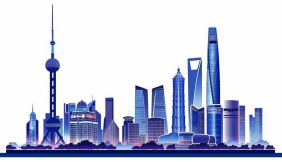
Paper Id	Topic	Title/Author
1195	2.9	SGFormer-RGCN: Accurate Performance Prediction for High-Level Synthesis Design Space Exploration *Ruiqi Tang, Shanshan Wang, Chenglong Xiao*
1442	2.9	RECALLS: Reinforcement Learning Enhanced Generative Model for Logic Synthesis Optimization *Ran Zhang, Xinda Chen, Rongliang Fu, Chunyang He, Da Wang, Fei Wang, Tsung-Yi Ho, Junying Huang*
1697	2.9	Reinforcement Learning Framework with Improved NSGA-II for Logic Synthesis *Zhiwei Tan, Jicong Fan, Zhongyan Xu, Xijun Cheng, Yufei Nai, Xiaofeng Gu, Zhiguo Yu*
2097	2.9	Sensitivity Analysis of Process Variables for Large-Scale Circuits Based on Graph Attention Networks *Zhe Zhu, Zhihao Li, Fei Li, Jun Tao*

Electronic Design Automation and Physical Design V Session

Session Code:	**A3P-24**	**Date & Time:**	**Monday May 25, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Xinfei Guo**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2180	2.9	TLMALS: Tiny Language-Model Enhanced ALS via Reinforcement Learning *Weichuan Zuo, Jienan Chen, Hongyi Wu, Yunlong Qi*
2344	2.9	Balancing Speed and Accuracy for Robust Analog-Mixed Signal Circuit Design Using Closed-Loop Reinforcement Learning with Ensemble Neural Network Surrogates *Zuwei Guo, Jie Fu, Sumukh Bhanushali, Zehua Zeng, Imon Banerjee, Arindam Sanyal*
2402	2.9	PhySeqForm: A Data-Driven, Physical Synthesis Sequence Former *Cunqing Lan, Zijian Jiang, Hongyang Pan, Zhiang Wang, Keren Zhu*
2666	2.9	An Efficient Optimization Framework for Netlist Partitioning by Co-Optimizing Moves and Replications *Qiwang Chen, Hailong You, Shunyang Bi, Zehong Wei*
2730	2.9	Library Index Optimization Through Diffusion Model for Accurate Timing Interpolation *Younggwang Jung, Chanjin Kim, Daijoon Hyun*
2401	2.9	EEschematic: Multimodal-LLM Based AI Agent for Schematic Generation of Analog Circuit *Chang Liu, Danial Chitnis*



Post-Quantum Cryptography and Cryptanalysis Session

Session Code:	**A3P-25**	**Date & Time:**	**Monday May 25, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Dur-e-Shahwar Kundi, Xinmiao Zhang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1054	3.8	A Scalable and Highly Efficient NTT Unit for CRYSTALS-Dilithium *Yuchen Wang, Xiaoke Wang, Kainan Ma, Chaoxing You, Shuang Xia, Ming Liu*
1122	3.8	HQC Post-Quantum Cryptography Decryption with Soft-Decision Reed-Solomon Decoder *Jiaxuan Cai, Xinmiao Zhang*
1662	3.8	A Unified Quantum Circuit Framework for Grover Search and Quantum Walks in NISQ Cryptanalysis *Leonardo Lavagna, Giacomo Vittori, Antonello Rosato, Massimo Panella*
2185	3.8	BRAM-Free ML-KEM NTT with SRL-Based Reordering Unit *Gijung Kim, Yongmin Park, Chae Eun Rhee*

Statistical Signal Processing Session

Session Code:	**A3P-26**	**Date & Time:**	**Monday May 25, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Xin Lou**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1317	10.5	Robust Floating Offshore Wind Turbines State Estimation Under Covariance Mismatch and Outliers with the Adaptive Fading Extended Kalman Filter *Jiatong Song, Shing Chow Chan*
1458	10.5	Model-Free Predictive Current Control of 2-Level Voltage Source Inverter via Robust Load Estimation in Impulsive Outliers *Xinyu Sun, Ting Liu, Shing Chow Chan, Ho Chun Wu*
1596	10.5	ICNet: Cross-Modality Image Analysis for IC Localization in Printed Circuit Boards *Jingyang Dai, Deruo Cheng, Xinrui Wang, Fei Ji, Yiqiong Shi, Bah Hwee Gwee*
2286	10.5	Robust Multichannel Autoregressive Parameter Estimation in Spatially Correlated and Impulsive Noise *Mingxi Lyu, Shing Chow Chan*
2916	10.5	Model-Free Predictive Current Control for PMSM Drives Using Extended State Observer *Ting Liu, Shing Chow Chan, Ho Chun Wu*

Signal Processing for Sensor Arrays and Wireless Communications Session

Session Code:	**A3P-27**	**Date & Time:**	**Monday May 25, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Qing Shen**

Papers are listed in the order they will be presented.

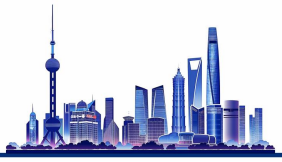
Paper Id	Topic	Title/Author
1009	10.6	A Low-Complexity Peak Search Method for Music Based on FFT and Early-Terminated Goertzel Algorithm *Ting Huang, Ziyu Guo, Jun Han, Xiaoyang Zeng*
1679	10.6	ISAC for Intelligent Transportation: Ray-Tracing, Clutter Cancellation, and Sensing-Aided Beamforming *Madhumitha Murthy, Hao Lin, Xiaojuan Zhang, Yonghong Zeng, Zhiping Lin, Yongming Chen, Francois Chin Po Shin, Sumei Sun*
2067	10.6	One-Bit DOA Estimation for Partially Calibrated Arrays with Unknown Uncertainties *Chenxi Liao, Qing Shen, Min Wang, Yuxiang Jiang, Youhao Kong, Wei Liu*
2068	10.6	Three-Dimensional Off-Grid Source Localization Based on Distributed Linear Array Networks *Yuning Peng, Qing Shen, Wei Liu, Yizhe Wang*
2432	10.6	A Non-Recovery Dynamic Range Efficiency Interference Cancellation Approach Based on Unlimited Sampling Framework *Yan Li, Chengbin Yang, Peng Zeng, Lei Qiu, Bin Wei*

Compute-in-Memory III Session

Session Code:	**A3P-28**	**Date & Time:**	**Monday May 25, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Ljiljana Trajkovic**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1004	14.1	SuperCIM: A Charge-Domain CIM with 3D Parallelism Reconfigurability Based on Asynchronous NoC Protocol *Yuxuan Ran, Tingran Chen, Bohan Xu, Biao Pan*
1008	14.1	Clipping Error Compensation for Accuracy Recovery and Throughput Improvement in Computing-in-Memory *Yu-Chih Tsai, Hsuan-Hung Shen, Ren-Shuo Liu*
1287	14.1	InFP: A 17.97 TFLOPS/W Reconfigurable SRAM Based Computing-in-Memory Macro for BF16 MAC Operations *Jing Zhang, Tianchu Dong, Shaoxuan Li, Zhengxi Yan, Shanshi Huang*
1323	14.1	Area-Efficient In-Memory Computing for Mixture-of-Experts via Multiplexing and Caching *Hanyuan Gao, Xiaoxuan Yang*
1451	14.1	RCW-CIM: A Digital CiM-Based LLM Accelerator with Read-Compute/Write *Yan-Cheng Guo, Tian-Sheuan Chang, Jian-Wei Su*
1106	14.2	A Fine-Grained Workload Orchestration Framework for Processing-in-Memory Architecture *Mengyuan Liu, Junpeng Wang, Song Chen*



Paper Id	Topic	Title/Author
1489	14.1	Energy-Efficient Compute-in-Memory Macro for BNNs in Edge AI Using NV-SRAM *Umme Hani Irin, Md Minhajul Azmir, Jinhui Wang, Md Rubel Sarkar, Yang Yi*
1737	14.1	A 66.15 TFLOPS/W RRAM-Based Near-Memory-Computing Macro Using Log-Multiplication and Error-Aware Adaptive Adder Structure with 2-D Pipelined CNN Dataflow *Yue-Ci Lee, Yuan-Ping Huang, Shyh-Jye Jou*
2312	14.1	GCC-CIM: A Charge-Domain Compute-in-Memory Macro Using Grouped-Row Capacitors and C-2C Ladder with Improved Multi-Bit MAC Linearity *Tong Wang, Erxiang Ren, Daniel Zheng Fang, Li Luo, Qi Wei, Fei Qiao*
2446	14.1	MDM: Manhattan Distance Mapping of DNN Weights for Parasitic-Resistance- Resilient Memristive Crossbars *Matheus Farias, Wanghley Martins, H. T. Kung*

Circuits and Algorithms for Visual Signal Processing Session

Session Code:	**A3P-29**	**Date & Time:**	**Monday May 25, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Yibo Fan**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1695	11.10	Enhancing SPAD HDR Imaging via Cross-Modality Frequency–Spatial Fusion *Yuhe Chen, Yunhui Zeng, Yue Xing, Xin Jin*
1711	11.11	MMCap: Multi-Level Clip Feature Fusion with Multiway Dynamic Dense Connections for Urban Incivility Scene Captioning *Yeping Zhao, Jian Ma, Jun Ma, Guohui Deng, Jinghan Wang, Guoming Xu*
2192	11.11	E2Detect: Object Detection from Event Camera via Sparse Feature Pyramid Recovery *Chris Henry, Zhu Li, Aggelos Katsaggelos*
2890	11.11	CADA: Chroma-Aware Denoising Architecture for Low-Light Raw Images *Liyuan Peng, Yujie Huang, Mingyu Wang, Xiaoyang Zeng*
1145	11.14	CIM-SIFT: An Efficient Compute-in-Memory Accelerator for Real-Time SIFT Algorithm *Zhengxi Yan, Cong Wang, Xipeng Lin, Jing Zhang, Hongwu Jiang*
1478	11.14	EdgeFER: A Structure-Guided and Hardware-Friendly Framework for Dynamic Facial Expression Recognition *Zhenting Zhou, Albert Chen, Asebe Teka Nega, Jianwen Chen*
1703	11.6	DocIQ: A Benchmark Dataset and Feature Fusion Network for Document Image Quality Assessment *Zhichao Ma, Fan Huang, Lu Zhao, Fengjun Guo, Guangtao Zhai, Xiongkuo Min*
2032	11.6	Vision-Language Modality Prompt Classification Method for Image Quality Assessment *Yongkang Hou, Jiarun Song*
1660	11.8	Binary Descriptor Learning via Diffusion-Based Feature Disentanglement *Shunan Mao, Gang Shen, Xuefei Lv, Ziwei Liu, Shiliang Zhang*

Datapath & Arithmetic Circuits and Systems III Session

Session Code:	**B1P-20**	**Date & Time:**	**Tuesday May 26, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Hao Zhang**

Papers are listed in the order they will be presented.

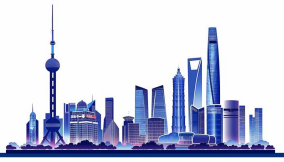
Paper Id	Topic	Title/Author
1714	2.1	A Low-Cost and High-Accuracy Bipolar Divider for Stochastic Computing *Shaowei Wang, Minghui Zhou, Jian Chen, Yi Wang, Yaohua Xu, Sheng Wang*
2028	2.1	A Multi-Precision Tensor Processing Unit for Accelerating Matrix Computations *Weijie Chen, Zongfan Wu, Dong Jiang, Enyi Yao*
2056	2.1	Silicon-Based Evaluation of CSD Arithmetic in a RISC-V Processor Using Open-Source ASIC Flow *Farhad EbrahimiAzandaryani, Michael Kupfer, Dietmar Fey*
2063	2.1	Static Segment-Based Approximate Booth Multiplier with Probabilistic Error Compensation *Dongxiao Yu, Yuhang Ren, Zhenyu Wang, Chen Qin, Lulin Cai, Yajuan He*
2141	2.1	FlexMulSim: A Full-Precision Hardware Reuse Simulator for Power, Area, and Utilization Efficiency *Jiangtao Cui, Xinyu Shao, Dongwei Xu, Sheng Zhang*

Datapath & Arithmetic Circuits and Systems IV Session

Session Code:	**B1P-21**	**Date & Time:**	**Tuesday May 26, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Yeong-Kang Lai**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2246	2.1	Efficient Top-K Sorter Through Runtime Lane Selection of Priority Queues on a Directed Ring *Huawen Liang, Wei Yuan, Qizhe Wu, Xi Jin*
2415	2.1	An Iterated Hybrid Fast Parallel FIR Filter *Keshab K Parhi*
2813	2.1	Triple-Packed Posit MAC: Low-Bitwidth Inference via Tri-Product DSP48E2 Overpacking for CNNs *Nishith Akula, Sujit Ghantasala, Sai Vishwanath Rohit Komaragiri, Rahul Mukundhan, Madhav Rao*
2711	2.4	A Membrane Potential Communication-Based Network-on-Chip for Merge-Core-Free Spiking Neural Network Deployment *Weilai Chu, Zhantao Liu, Chongyang Li, Youming Liu, Chenyang Liu, Pujun Zhou, Guanchao Qiao, Shaogang Hu*
2910	2.4	GTPE: A 28nm 33.12 TFLOPS/W GNN Training Processor with Unstructured Multi Threshold Pruning, Hybrid Multi-Mode Approximate Computing and QUIRE Number System Support *Zhou Wang, Haochen Du, Zhou Shu, Jiuren Zhou, Xiguang Wu, Qiankun Li, Yanqing Xu, Hanqi Feng, Xiaonan Tang, Shushan Qiao, Tianchun Ye, Yang Liu, Anil A. Bharath, Emm Mic Drakakis*



SoC, NoC, Multi-Core, and 3D/2.5D Integrated Circuits and Systems III Session

Session Code:	**B1P-22**	**Date & Time:**	**Tuesday May 26, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Bo Wang, Lan-Da Van**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1288	2.4	Thermal-Aware 3D-IC Floorplan Based on TSV-Coordination Simulated Annealing *Xingjie Zou, Wenbo Zhang, Linfeng Wu, Heng Zhang, Xinyu Wang, Yuxiang Fu, Li Li*
1606	2.4	An Efficient BIST and Fault Diagnosis Circuit for TSVs *Guowei Xing, Xiaowen Jiang, Pengkang Luo, Zhenming Li, Wei Xi, Kai Huang*
1807	2.4	HOC: Hierarchical Overlapped Communication Optimization for Parallelism in Distributed Training *Zeyue Wang, Yuanyuan Wang, Shu Pan, Yuyang Wang, Nana Tang, Fei Yang*
2218	2.4	Topology-Mapping Co-Design for Scalable LLM Accelerators with Hierarchical Mesh-of-Trees NoC *Zhen Wu, Yimin Wang, Yue Jiet Chong, Xuanyao Fong*

Error Correction Codes and Secure Communication Hardware Session

Session Code:	**B1P-23**	**Date & Time:**	**Tuesday May 26, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Youngjoo Lee**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1103	3.10	Design and Implementation of a Low Latency and Low Complexity Reed-Solomon Decoder for IEEE 802.15.4a/z IR-UWB *You-Jie Siao, Chung-An Shen*
1384	3.10	Compact Inverter-Triggered SCR for ESD Protection in Broadband Communication Circuits *Hao-Yuan Lee, Hao-En Cheng, Chun-Yu Lin*
1572	3.7	High Throughput LDPC Decoder with Ultra-Low BER Using Hardware Sharing Across Two Code Rates for IEEE Std. 802.15.3d *Ching-Liang Yeh, Yi-Shan Huang, Chung-Lun Tu, Shyh-Jye Jou*
2193	3.8	Securing IoT with True Randomness and Side-Channel Resistant ECC: A Layered Hardware-Software Approach *Michael Nascimento, Edward Moreno, Calebe Conceição*

Energy-Aware and Resilient Communication Systems Session

Session Code:	**B1P-24**	**Date & Time:**	**Tuesday May 26, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Joungsun Park**

Papers are listed in the order they will be presented.

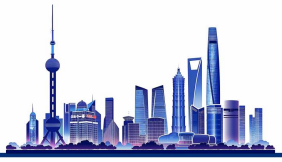
Paper Id	Topic	Title/Author
1226	3.10	Experimental Evaluation of a Varactor-Tuned Programmable Metasurface with Modular Electronics – Toward ASIC Integration *Loukas Petrou, Konstantinos Michail, Anastasis Kounoudes, Marco A. Antoniades, Julius Georgiou*
1255	3.3	An 80 Gbit/S NRZ 100 Gbit/S PAM4 Highly-Efficient Voltage-Mode VCSEL-Driver in 22nm FDSOI CMOS *Nikolaos Kioulos, Urs Hecht, Helia Ordouei, Nikolay Ledentsov Jr., Sebastian Linnhoff, Si-Cong Tian, Friedel Gerfers*
2541	3.9	An Ultra-Low-Power IR-UWB Energy-Harvesting Tag for Unsynchronized Multi-User Transmission *Patrick Fath, Harald Pretl*
1405	15.11	A 56Gb/s PAM-4 Transmitter with Robust DCC and Unsegmented Voltage-Mode Driver Achieving Wide-Coefficient-Tuning-Range FFE in 65nm CMOS *Lihong Yang, Zhongji Zhang, Xiaoteng Zhao, Zhao Song, Zixing Luo, Zhangming Zhu*
1978	15.5	Accurate Localization of RF Signals Based on Adaptive Normalized SR System and Phase Estimation *Qichang Yong, Di He*

CAS Education and Outreach: Teaching Methods and Tools Session

Session Code:	**B1P-25**	**Date & Time:**	**Tuesday May 26, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Vasilis Ntinas, Abderazek Ben Abdallah**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1065	13.1	Exploring the Practice-Driven Learning Model with the Buck Converter Experiment *Hua Fan, Yue Shu, Lishuang Lin, Panfeng Zhao, Wei Zhou*
1121	13.4	RISC-V and SHA-256 Accelerator Hackathon: A Problem-Based Learning Approach to Hardware-Software Co-Design *Freddy Gabbay, Sarit Shvimer, Alex Grinshpun*
1538	13.6	A Challenge-Based-Learning System to Improve Education in Circuit and System Design *Dominik Zupan, Jan Eberl, Colin Pluns, Bernd Deutschmann*
1813	13.5	Educational Perspectives on LLM Architectures: Analyzing Code Generation for Circuits and Systems *Rupesh Raj Karn, Johann Knechtel, Ozgur Sinanoglu*
2947	13.3	Embedding Passion: A Project-Based Scaffolding Framework for Embedded Systems Education *Qingqing Ni, Linxin Hou, Jing Gu, Henry Tan, Ankit Srivastava, Christopher Moy, Chen Khong Tham, Rajesh Panicker*
2633	13.5	A Time-Domain Verification Framework for Digitally-Trained Op Amp and Ring-Oscillator Based Analog Spiking Neural Network *Sai Sanjeet, Bibhu Datta Sahoo*
2935	13.1	No Gate-Keeping: Teaching Novice Engineering Students to Build a CPU on FPGA *Neil Banerjee, Si Wang, Rajesh Panicker*



Neural Learning and Perception Systems I Session

Session Code:	B1P-26	Date & Time:	Tuesday May 26, 2026 (10:00 - 12:00)
Location:	SHICC Lobby, Level 3	Chair:	Yuncheng Lu

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1237	8.1	A Multiplier-Free Similarity Metric for Token Merging in Vision Transformers *Yupeng Gui, Ruiqi Tang, Shichen Peng, Han He, Sheng Zhou, Leilei Huang, Xiao Yan, Yibo Fan*
1740	8.1	Federated LoRA with Fixed Orthogonal Basis and Dimension-Wise Aggregation *Jiankun Liu, Qi Li, Xiaoyan Gu, Jing Yu, Chi Chen, Weiping Wang*
2199	8.1	Empirical Study of Process Reward-Guided Model Ensemble for Edge Reasoning *Yide Liu, Yuqi Wu, Shengming Zhao, Tianyi Ye, Jie Chen*
2507	8.1	Dynamic GNNs for Continual Learning on Circuits *Rupesh Raj Karn, Johann Knechtel, Ozgur Sinanoglu*
1776	8.1	Single-Pass Anchor-Based Uncertainty Quantification in Deep Neural Networks *Dimitrios Spanos, Nikolaos Passalis, Anastasios Tefas*
1995	8.8	Energy Function Choice for Training Nonlinear Resistive Neural Networks with Equilibrium Propagation *Zülal Kiraz, Dang-Kiên Germain Pham, Patricia Desgreys*

Neural Learning and Perception Systems II Session

Session Code:	B1P-27	Date & Time:	Tuesday May 26, 2026 (10:00 - 12:00)
Location:	SHICC Lobby, Level 3	Chair:	Chang Gao

Papers are listed in the order they will be presented.

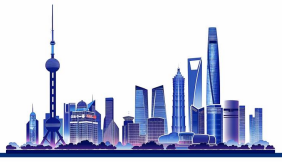
Paper Id	Topic	Title/Author
1286	8.1	Urban Traffic Short-Term Flow Prediction Based on the Fusion of Multiple Correlations *Qiang Ai, Min Yuan*
1517	8.1	Screen-Shooting Resilient Watermarking Based on Perceptual Mask-Guided Embedding and Feature-Segmentation Decoding *Yan Zhou, Gang Shi*
1864	8.4	Memory-Efficient In-Sensor Event Denoising with a Lightweight Point-Cloud Network *Zongpei Fu, Xiaojin Zhao, Wenbin Ye*
2271	8.3	A Near-Sensor Image Compression Architecture with RRAM-Based Hyperdimensional Encoder for Smart Vision *Haoyang Gu, Zheng Zhou, Zongwei Wang, Jinshan Li, Zezhi Chen, Ling Liang, Wengao Lu, Yimao Cai*
1077	8.1	ElecThinker: A Three-Stage Framework to Enhance Electronic Diagram Reasoning in Multimodal LLMs *Qirui Chen, Qirui Bai, Dong Jin, Jiangming Li, Jun Chen, Shuangwu Chen, Shenghao Ye, Wangming Li*
1677	8.1	SCASN: Sparse Cross-Attention Self-Supervised Network for Endoscopic Surgical Video Desmoking *Wanyi Zhou, Yinna Zhu, Zijing Zhang, Gengsheng Chen, Wei Xu, Zhenyang Li, Meng Shi*

Quantization, Approximation, and Compression for ML Hardware III Session

Session Code:	**B1P-28**	**Date & Time:**	**Tuesday May 26, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Bokyung Kim**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1900	14.3	A Low-Error Approximate Logarithmic Multiplier with Symmetric LUT for Efficient DNN Training *Xudong Zheng, Baoting Li, Tai Yu, Hang Wang, Xuchong Zhang, Hongbin Sun*
2205	14.3	Composit: A Dual-Precision Posit MAC and a Composite Quantisation Scheme for Accelerated Mixed-Precision Neural Network Inference *Shruti Singh, Aravind Voggu, Madhav Rao*
2300	14.2	Approximate DCT Using Scaling Factor Optimization for Error-Resilient Applications *Pranav Kumar VS, Lakshmi Soumya Burle, Shylashree N, Viveka Konandur Rajanna*
2701	14.1	A Compute-in-Memory Based on Approximate Multiplication with a Calibration Adder *Seunggu Choi, Minkyu Song, Soo Youn Kim*
2817	14.1	A Synthesizable Mixed-Precision DCIM Macro with Parallel Write and Compute *Jinane Bazzi, Mohammed Fouda, Ahmed Eltawil*
1223	14.2	Adaptive Row-Wise Attention Score Pruning and Compensation for Attention Acceleration *Chia-Chun Wang, Yu-Lin Lin, Ren-Shuo Liu*
2438	14.2	A Unified Function Processor with Integer Arithmetic Based on Piecewise Chebyshev Polynomial Approximation *Xiaoyu Zheng, Ziyi Guo, Changchun Zhou*
2799	14.2	MPE: A Power-Efficient Edge-Device Mamba Processor with Multi-Dimensional Calculation-Compression Scheme *Zhou Wang, Haochen Du, Zhou Shu, Jiuren Zhou, Xiguang Wu, Qiankun Li, Yanqing Xu, Hanqi Feng, Xiaonan Tang, Shushan Qiao, Yongke Wang, Yang Liu, Anil A. Bharath, Emm Mic Drakakis*
2911	14.2	MEGA.mini-S: A 1.9-to-15.0 TOPS/W Generative AI Processor with Bit-Serial Weight Scalability and Bank-Conflict-Free Sparsity Compression *Taesu Kim, Donghyeon Han*
1427	14.3	A Hardware-Software Co-Design for LLMs with Exponent-Element Quantization Towards Compute-in-Memory *Qining Zhang, Aoyun Feng, Hongfei Ye, Jianhua Feng*



Noise-Shaping SAR ADCs Session

Session Code:	**B3P-17**	**Date & Time:**	**Tuesday May 26, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Joseph Chang, Thierry Taris**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1621	1.3	A 98.3dB-SNDR 100kHz-BW 4th-CIFF Noise-Shaping SAR ADC Using Source Degeneration Floating Inverter Amplifier *Longjiang Jia, Yuanhong Ding, Zhongwei Lin, Yushan Dai, Jian Mei, Lei Deng, Rui Yin*
2075	1.3	A 14.3-ENOB, 600-kHz BW Third-Order NS-SAR ADC with Enhanced EF-CIFF Filter *Zhenxing Li, Jiaqi Tang, Changze Yu, Yishan Wang, Yongkui Yang*
2116	1.3	A 16- ENOB 2nd Order Noise-Shaping SAR ADC with Mismatch Error Shaping and Optimized Switch Charge Injection Balancing *Ziang Shen, Yang Zhao, Yong Lian*
2323	1.3	A 185 dB FoMS Direct-Integration Third-Order Passive Noise-Shaping SAR ADC for Biomedical Applications *Kangkang Sun, Kailin Lin, Weijie Ge, Feng Yan, Bingjun Xiong, Jian Guan, Jingjing Liu*

High-Speed and Precision SAR ADCs Session

Session Code:	**B3P-18**	**Date & Time:**	**Tuesday May 26, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Xi Zhu, Jorge Fernandes**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1474	1.3	A 16-Bit SAR ADC with kT/C Noise Cancellation Using Nested Auto-Zero *Yuzhou Liu, Kejun Wu, Zhong Zhang, Ruixin Li, Zhengye Jin, Shengxin Wang, Xiaoqian He, Zhen Yu, Ning Ning, Jing Li, Qi Yu*
1704	1.3	A 7-Bit 1-GS/s Single-Channel Partial Loop-Unrolled SAR ADC Featuring Constant Input Common-Mode for Comparators in 28-nm CMOS *Shipeng Zhang, Cheng Yuan, Qiuwei Wang, Wenting Wang, Yao Li, Mao Ye, Yong Chen*
2095	1.3	An Energy and Area-Efficient Ternary SAR ADC with Tri-State Comparison *Tianci Zhang, Shengrui Chen, Zhangyuan Xie, Dongxu Li, Yihu Yu, Zhong Zhang, Kejun Wu, Ning Ning, Qi Yu, Jing Li*
2470	1.3	A 12-Bit 5-MS/s TMR-Free Radiation-Adaptive SAR ADC for Space Missions with 67.55-dB SNDR in 22-nm FD-SOI *Jinghao Zhao, Zheyi Li, Qichao Ma, Qiuyang Lin, Yihong Qing, Xingfa Zheng, Maxim Gorbunov, Bo Gao, Chaohan Wang, Mingzi Zhang, Esmee Tackx, Jeffrey Prinzie, Paul Leroux*
2635	1.3	A 7-Bit 1-GS/s Single-Channel Charge-Injection Loop-Unrolled SAR ADC with Foreground Calibration *Cheng Yuan, Shipeng Zhang, Wenting Wang, Qiuwei Wang, Mao Ye, Yong Chen*

Pipelined and Time-Interlaved ADC Techniques Session

Session Code:	**B3P-19**	**Date & Time:**	**Tuesday May 26, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Cindy Tam, Tawfiq Musah**

Papers are listed in the order they will be presented.

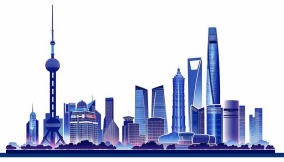
Paper Id	Topic	Title/Author
1239	1.3	A 4GS/s 8b Time-Interleaved SAR ADC with LSB-Repeating-Based Background Offset Calibration and Adaptive-Average Residue Estimator *Yunsong Tao, Xiyu He, Yuxuan He, Jun Bai, Xiaoge Zhu, Anqiang Guo, Hao Luo, Long Kong, Shaodi Wang, Yi Zhong, Lu Jie, Nan Sun*
1247	1.3	Spectral Impact of Mismatches in Interleaved ADCs *Jérémy Guichemerre, Robert Reutemann, Thomas Burger, Christoph Studer*
1311	1.3	An Inter-Channel Calibration Technique for the Correction of All Static Errors in SAR ADCs *Enrico Miotello, Amrith Sukumaran, Stéphane Emery, Taekwang Jang*
2147	1.3	A PN-Assisted Dynamic-Window Interstage Gain Calibration for Pipeline-SAR ADCs *Li Dang, Chengyuan Liu, Yue Cao, Hongzhi Liang, Ruixue Ding, Shubin Liu, Zhangming Zhu*
2617	1.3	An 89.3 dB SNDR MASH 1-2 Pipelined SAR ADC Using Stacking FIA with Extended Voltage Domain *Renzhen Liang, Qiaoyu Hu, Yuchen Liu, Yuke Shen, Yanbo Zhang, Zhangming Zhu*

Low-Power Logic, Circuits & Architectures IV Session

Session Code:	**B3P-20**	**Date & Time:**	**Tuesday May 26, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Chung-An Shen**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1175	2.2	Hybrid Dynamic/SRAM Based TCAM Cell with Self-Gating Match Line and Adaptive VSS *Xie He, Zuqi Zhang, Zeyu Liu, Chenghe Sun, Xiangyi Chu, Rui P. Martins, Pui-In Mak, Jiawei Xu*
1388	2.2	Probabilistic-Based Complementary Logic Gate Design *Yufeng Li*
1401	2.2	A 2-GHz 5.06-mW Phase Accumulator Employing Dynamic Regulation for High-Speed Direct Digital Frequency Synthesizers in 65-nm CMOS *Bin Kong, Kai Cheng, Hongyu Ren, Xianghe Meng, Xiaoyu Shan, Yunbo Huang, Li Wang, Zunsong Yang, Bo Li*
1499	2.2	A Stable Approximate Pruning Framework with Heuristic Optimization *Lulin Cai, Dongxiao Yu, Pufan Luo, Benhao Pan, Yajuan He*
2206	2.2	XHDC: An Adaptive Hyperdimensional Computing Accelerator with Incremental Learning *Ruofan Yan, Changzhen Han, Hao Xu, Ke Chen, Weiqiang Liu*



Low-Power Logic, Circuits & Architectures V Session

Session Code:	**B3P-21**	**Date & Time:**	**Tuesday May 26, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Huiyun Li**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2590	2.2	An Ultra-Low Power Data Retention Flip-Flop with 25.8 pW Leakage in 28 nm CMOS *Guangnan Dai, Yihan Zhang*
2677	2.2	A High-Compression SISO CNN Accelerator Chip for Low External Memory Access *Jing Shiun Hu, Qi Hua Lin, Che-Wei Lin, I-Chyn Wey*
2776	2.2	An Efficient Sine/Cosine Design Using Piecewise Quadratic Approximation for FOC Applications *Yitong Wang, Yuan Gao, Yuan Cao, Jianjun Zhuang, Zhao Huang, Rongkai Pan, Jing Tian*
2863	2.2	Power-Efficient and Reconfigurable Compute Unit for Multi-Precision AI Inference at the Edge *Muhammad Hamis Haider, Hao Zhang, Seokbum Ko*
2883	2.2	Implementation and Evaluation of a Cryogenic DSP in 22-nm with Floating-Point Arithmetic for Estimating Qubit States *Yuki Koyama, Takashi Imagawa, Ryo Kishida, Takefumi Miyoshi, Kazutoshi Kobayashi*

Design and Verification of Digital Integrated Circuits and Systems III Session

Session Code:	**B3P-22**	**Date & Time:**	**Tuesday May 26, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Tian-Sheuan Chang, Meiqi Wang**

Papers are listed in the order they will be presented.

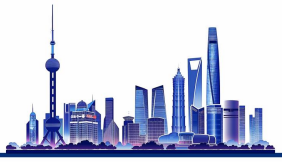
Paper Id	Topic	Title/Author
1141	2.10	MILEAM: Modeling Input-Aware Logic Errors of Approximate Multipliers Using Machine Learning *Jinghao Wen, Dongning Ma, Xun Jiao*
1262	2.10	IDIM: In-Situ DRAM-Based Ising Machine with All-to-All Connectivity *Wenya Deng, Zhi Wang, Yingzhe Luo, Junwei Zeng, Sheng Liu, Xiaowen Chen, Yang Guo*
1506	2.10	FinFET-Based High Performance Radiation-Hardened SRAM Cell Design with Optimized Layout for Commercial Aerospace *Minchi Hu, Xuezhi Zheng, Jing Zhang, Zhehan Dang, Lei Shen, Chang Cai*
1597	2.10	A Co-Design Architecture for Synergistic Mitigation of SEL and SEU in 16 nm FinFET-Based Radiation-Hardened SRAM *Xuezhi Zheng, Minchi Hu, Mingzhang Duan, Zongxuan Xie, Hongjie Zeng, Xiang Wang, Zejun Li, Chang Cai*

Nanoelectronic Devices and Circuits Session

Session Code:	**B3P-23**	**Date & Time:**	**Tuesday May 26, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Hao Cai**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2391	5.1	High-Speed and Low-Power Graphene ADC with Scalable Resolution *Nicoleta Cucu Laurenciu, Charles Timmermans, Sorin Cotofana*
2475	5.2	A Vertically Stacked CMOS-MEMS Temperature/Humidity Sensor System for Real-Time Respiration Monitoring *Mengliang Jia, Linze Hong, Minghan Li, Ruining Xu, Wei Xu*
1943	5.4	A 3.4-MHz Class-A Operational Amplifier in GaN Monolithic Technology with 80 dB Open-Loop Gain *Abhishek Joarder, Andrea Gambero, Sandro Rossi, Giulio Ricotti, Antonio Aprile, Edoardo Bonizzoni, Piero Malcovati*
1093	5.6	RRAM-as-Reference Sensing with Parallelogram Crossbar Architecture for Large-Scale Arrays *Running Guo, Stefan Pechmann, Andrea Baroni, Eduardo Pérez, Christian Wenger, Pengcheng Xu, Amelie Hagelauer*
1314	5.6	64-Point Radix-4 Fast Fourier Transform (FFT) Implementation in an 8 × 4 1T1R RRAM Array *Siyuan Jia, Xiaohua Liu, Rainer Waser, Stefan Wiefels, Stephan Menzel*
1681	5.6	An Efficient On-Chip Adaptation Technique for MAML Models on Memristive Hardware *Aabid Amin Fida, Sparsh Mittal*
2087	5.6	Variability Aware Design of Memristor-Based Gene Implementation in Cellular Neural Networks *Ahmed Magdy Abdelsamad, Vasileios Ntinas, Dimitrios Prousalis, Ioannis Messaris, Ahmet Samil Demirkol, Vikas Rana, Stephan Menzel, Alon Ascoli, Ronald Tetzlaff*
2294	5.6	Memristive Probabilistic Neuron Enhanced Memristor-Based Ising Machine for Efficient Combinatorial Optimization *Zhoujie Pan, Yanming Liu, Peigen Zhang, He Tian*
2296	5.6	A Front-End for Parkinsonian Tremor Detection Using Memristive Spike Encoding *Ioannis K. Chatzipaschalis, Ioannis Tompris, Iosif-Angelos Fyrigos, Antonio Rubio, Georgios Ch. Sirakoulis*
1973	5.9	A Yield-Enhanced and Highly Reliable 512k-Bit HZO-Based 2T2C FeRAM Chip Enabled with Charge Pump *Xiangyin Chen, Jing Wang, Yangtong Yu, Zhongguang Xu*
2518	5.9	CIMA: An Energy-Efficient In-Memory Accelerator Architecture Based on Non-Volatile Capacitive Crossbar Array for Random Forest Inference *Jinrong Zhou, Shaoan Yan, Jianjun Chen, Bin Liang, Zhuojun Chen*



Spintronic and Quantum Circuits Session

Session Code:	**B3P-24**	**Date & Time:**	**Tuesday May 26, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Kyeong-Sik Min**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1354	5.5	An Edge-Pursuit Ising Machine with Programmable Local Fields and Adaptive Annealing *Bocheng Xu, Jiahao Song, Zihan Wu, Xiyuan Tang, Xiaochen Bo, Yuan Wang*
1595	5.5	Fully Parallel Ising Machine with MRAM Based p-Bit Probabilistic Simulated Annealing *Tianhao Chen, Tianqu Hu, Shan Yao, Chengshuo Yu, Tianxiao Nie, Xufeng Kou*
1805	5.7	Generic Cryogenic VLSI Design Flow and Optimization Strategies for Energy-Efficient Computing *Yumeng Yuan, Chang He, Yue Xin, Kagan Irez, Zewei Wang, Xufeng Kou*
2186	5.5	A Highly-Scalable and Full-Connected SOT P-Bit Ising Annealer for Combinatorial Optimization *Huanghui Wang, Haoran Du, Yantong Di, Zeying Ding, Jiongzhe Su, Jingchao Zhang, Miao Yu, Xin Si, Bo Liu, Yan Cui, Hao Cai*
2264	5.5	Design and Implementation of a Scalable 64 p-Bits Ising Computing Chip with Integrated SOT-MTJs for Efficient Computing *Boyan Zhang, Jinhao Li, Yuan Wang, Jialiang Yin, Linying Liu, Hongchao Zhang, Chengyuan Sun, Hong-Xi Liu, Xuan Li, Kaihua Cao, Zhaohao Wang, Wenlong Cai, He Zhang*
2295	5.5	A Half-Cell-Activation Search Scheme for Low-Power and High-Reliability TCAM Design *Qingting Hu, Erya Deng, Jiaqi You, Hao Kang, Guanyu Zhao, Weiqiang Liu*
2413	5.7	A 40 nm Integrated Cryo-CMOS 120 MHz Switching Power Converter for Power Management at 4 K Aiming Large-Scale Quantum Computers *Xavier Íñiguez Fainé, Eduard Alarcón, Fabio Sebastiano, Llorenç Fanals-I-Batllori, Aldo Pena Perez*
2460	5.5	Hybrid-Domain STT-MRAM Compute-in-Memory Scheme for Quantized Deep Neural Network *Haoran Du, Tingxuan Shi, Shuyu Wang, Hongjin Zhu, Huanghui Wang, Zeying Ding, Yantong Di, Bo Liu, Hao Cai*
2503	5.5	A 0.562 mm² MTJ-Based Ising Machine for 48-Bit Integer Factorization in 40 nm CMOS *Kunpeng Gao, Jiadong Chen, Yifan Wang, Shao Hao Wang, Tai Min, Yufeng Xie*
2719	5.5	Highly Energy-Efficient In-Memory Computing Architecture Based on VGSOT-MRAM for Reconfigurable BNN/TNN Acceleration *Qihang Gao, Chao Wang, Chenghang Li, Zhongzhen Tong, Zhaohao Wang*
2990	5.5	Dual 3T2R Differential SOT MRAM Array for Energy-Efficient In-Memory Computing in Deep Reinforcement Learning *Yiyuan Xiao, Cancheng Xiao, Bingqian Song, Jiahao Zhao, Yining Li, En Li, Baiyu Su, Jianshi Tang, Tianxiang Nan*
1962	5.7	CLOAQ: Combined Logic and Angle Obfuscation for Quantum Circuits *Vincent Langford, Shihan Zhao, Hongyu Zhang, Ben Dong, Qian Wang, Anees Rehman, Yuntao Liu*
2679	5.7	Cryo-CMOS Antenna for Wireless Communications Within a Quantum Computer Cryostat *Viviana Centritto, Ama Bandara, Heqi Deng, Masoud Babaie, Evgenii Vinogradov, Sergi Abadal, Eduard Alarcón*

Modeling Methods for Nonlinear Circuits and Systems II Session

Session Code:	**B3P-25**	**Date & Time:**	**Tuesday May 26, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Ben Cheng**

Papers are listed in the order they will be presented.

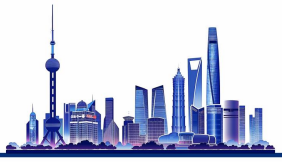
Paper Id	Topic	Title/Author
1444	9.5	Adaptive-Fusion Particle Filter with Distributed Resampling and Dynamic Particle Scaling *Shuanglong Liu, Xiaowei Wang, Botong Zhou, Wenjun Luo, Jia Liu, Jiaqi Ma*
2187	9.6	A Comparative Study of Real-Time Learning Algorithms for Multiband Digital Predistortion Using LTE/5G Signals *Zixiao Yang, Smail Bachir, Claude Duvanaud*
2620	9.10	An AI-Based Pareto-Driven Cost-Dimension Optimization of EMI Filters for DC-DC Converters *Lorenzo Nikiforos, Francesco Gabriele, Fabio Pareschi, Gianluca Setti*
2628	9.6	Radiation-Hardened Circuit for Chaos-Based Characterization of Cosmic Ray Dynamics in Space Missions *Elias de Almeida Ramos, Augusto Weber, João Baptista Martins, Ricardo Reis*

Modeling Methods for Nonlinear Circuits and Systems III Session

Session Code:	**B3P-26**	**Date & Time:**	**Tuesday May 26, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Yujiao Dong**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1396	9.1	Analogue Studies of Energy Recurrence in Fermi–Pasta–Ulam–Tsingou Systems *Hao Qian, Zidu Li, Bhaskar Choubey*
2008	9.7	A Low-Complex and Dual-SPSA Digital Predistortion for MIMO Transmitters with Crosstalk *Rui Zhou, Yufeng Wu, Jiayin Song, Wulve Yang, Wei Wu, Yi Zhan, Shushan Qiao*
2027	9.9	Data-Driven Parameter Design Method for Memristive LIF Neuron Circuits *Yan Liang, Lei Chen, Yujiao Dong, Yidan Mao, Yue Jiang, Ciyan Zheng*
2421	9.1	Load Impedance Matching for Kinetic Energy Harvesters Operating Under Displacement Constraint *Moein Rahmani, Armine Karami, Dimitri Galayko, Philippe Basset*



Robustness and Security in Vision and Generative Models Session

Session Code:	**B3P-27**	**Date & Time:**	**Tuesday May 26, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Yuanman Li**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1261	12.4	A Collaborative Adversarial Purification Framework with Perturbation-Insensitive Semantics-Guidance *Kaifeng Chen, Peisong He, Lei Zhang, Haoliang Li, Ke Xu*
2303	12.12	Adversarially Regularized Latent Flow for Enhanced Conditional Video Generation *Jinduo Wang, Zhi Lu, Binquan Wang, Dongheng Zhang, Yang Hu, Yan Chen*
2305	12.4	Lightweight Recaptured Image Detection Model with Gradual Unfreezing and Structured Pruning *Oussema Feki, Wissem Karous, Aymen Hamrouni, Hakim Ghazzai, Saber Feki, Gianluca Setti*
2888	12.4	Malice Hides in Equivalence: Attacking Text-Image Alignment Assessment with Subtle Text Variations *Kang Xiao, Xuelin Shen, Baoliang Chen, Wenhan Yang, Li Zhang, Meng Wang*

Multimodal Intelligence for Visual Restoration and Generation Session

Session Code:	**B3P-28**	**Date & Time:**	**Tuesday May 26, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Xiangyu Chen**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1644	12.12	Audio-Visual Synergy for High-Fidelity Portrait Animation: A Two-Stage Framework with Identity-Motion Disentanglement *Yuzhi Lu, Yuanzong Mei, Wenyi Wang, Xi Chen, Xiaowen Chen, Zhi Wang, Feng Xu, Jianwen Chen*
2730	12.15	Energy-Aware Heterogeneous Deployment of Learned Image Codecs *George Paul, Robert Nicol, Boguslaw Obara, Deepayan Bhowmik*
1965	12.11	Interactive State Space Model with Cross-Modal Local Scanning for Depth Super-Resolution *Chen Wu, Ling Wang, Zhuoran Zheng, Xiangyu Chen, Jingyuan Xia, Weidong Jiang, Jiantao Zhou*

Readout and High-Speed Interface Circuits Session

Session Code:	**C1P-17**	**Date & Time:**	**Wednesday May 27, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Navid Yazdi, Zhishuai Zhang**

Papers are listed in the order they will be presented.

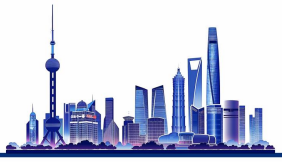
Paper Id	Topic	Title/Author
1181	1.4	A Low Power Single Sampler Based PAM3 Error Receiver Using Incoming Error Signal Information *Raghavendra Rukmani Gowrishankar, Kamlesh Satyadev Singh*
2059	1.4	A Two-Stage Capacitive Readout ASIC for High-Resolution Surface Characterisation with Adaptive Tuning *Maryam Habibollahi, Arthur Jaccottet, Antonio Gomez, Nader Saffari, Andreas Demosthenous*
2227	1.4	A 20 Gb/s All-Digital CDR with Fast Locking and Improved Pi Linearity Using an Injection-Locked Ring Oscillator *Jimin Kim, Taeuk Kim, Jinwook Burm*
2572	1.4	A Digitally Controlled Delay Line with Delay Calibration in Phase-Interpolator *Arimu Kojima, Kenshin Sakaguchi, Shinya Nagasaki, Takefumi Yoshikawa*

Sample-and-Hold and Reference Circuits Session

Session Code:	**C1P-18**	**Date & Time:**	**Wednesday May 27, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Yi Zhong, Salvatore Pennisi**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1318	1.5	A Complete Low-Duty-Cycle S/H System with 100ms Hold Time at 175°C *Lorenzo Pulcini, Paolo Del Croce, Andrea Baschirotto*
2120	1.5	A Sub-50-nW Resistor-Less CMOS Current Reference Utilizing High-PSRR Voltage Biasing *Daokang Liu, Wenxin Zhao, Hainan Liu, Jiajun Luo, Bo Li*
2370	1.5	An All-MOS 1-nA Current Reference Insensitive to Process and Voltage Variations *Kexin Shan, Jiaqing Rui, Yuting Wan, Wenxian Gu, Xing Wu, C.-J.Richard Shi, Liangjian Lyu*
1429	1.5	An 8.91 nW, 1.74 ppm/°C Subthreshold CMOS-Only Voltage Reference for Temperature Sensors *Bingjun Xiong, Feng Yan, Weijie Ge, Kangkang Sun, Zhipeng Li, Jian Guan, Jingjing Liu*
1464	1.5	A 0.5V 72-pW Process and Temperature Compensated Voltage Reference *Vikkram Srinivasan, Damini Chandi Priya Adusumilli, Ashfakh Huluvallay, Arpan Jain, Abhishek Pullela, Andleeb Zahra, Zia Abbas*



Comparators and Time-Based Circuits Session

Session Code:	**C1P-19**	**Date & Time:**	**Wednesday May 27, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Jerald Yoo**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1016	1.3	Analytical Derivation of Quantization Error in Threshold Level Quantizers Using Bipolar PFM *Ricardo Carrero, Ruben Garvi, Luis Hernandez*
1565	1.8	A High Full-Scale Range High-Linearity 9.76-Ps Resolution Time-to-Amplitude Converter for TCSPC Applications *Jin Hu, Peishan Wang, Yang Liu, Xiayu Wang, Dong Li, Rui Ma, Zhangming Zhu*
1868	1.8	A Charge-Reusing Architecture for Low-Power StrongARM Latch Comparators *Francisco Simplício, Gonçalo Rodrigues, Jorge Fernandes*
1967	1.8	A Low-Noise Adiabatic Energy Recovery Dynamic Comparator with Complementary Gain-Boosting Preamplifier and Push-Pull Latch *Zhaoyi Liu, Krishna Dandavate, Srihari Hulugundi, Adyant Balaji, Johannes Leugering, Jiahao Song, Gert Cauwenberghs*
2763	1.3	An Elzakker Dynamic Comparator with Improved Speed and Rejection to Meta-Stability *Chunfeng Bai, Jiahang Xu, Tao Ma*

Hardware Security for Logic, Circuits and Architectures IV Session

Session Code:	**C1P-20**	**Date & Time:**	**Wednesday May 27, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Hui Chen**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1514	2.7	A Memory-Efficient NTT Accelerator with a Highly Parallel Memory Mapping Scheme *Hengyu Ding, Houran Ji, Jia Li, Jinhang Chen, Chiu-Wing Sham, Yao Wang*
1712	2.7	SilentBite: A Novel LLM-Based Framework for Automated Hardware Trojan Insertion *Shresth Shankhdhar, Ansh Bharadwaj, Vishesh Mishra, Sparsh Mittal*
2209	2.7	RASLL: A Removal Attack on SAT-Resistant Logic Locking *Zijian Long, Juncheng Chen, Han Zhang, Tong Lin, Aung Kyaw Nay, Bah Hwee Gwee*
2233	2.7	Graph-Structure-Aware Hyperdimensional Computing for Hardware Trojan Detection *Zilong Su, Fei Lyu, Yongjun Xia, Chenghua Wang, Yijun Cui, Weiqiang Liu*

Hardware Security for Logic, Circuits and Architectures V Session

Session Code:	**C1P-21**	**Date & Time:**	**Wednesday May 27, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Hui Chen**

Papers are listed in the order they will be presented.

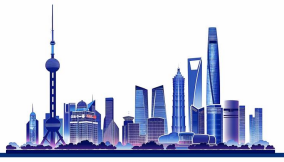
Paper Id	Topic	Title/Author
1811	2.10	AssertSynth: LLM-Based Assertion Synthesis via Multimodal Specification Extraction *Enyuan Tian, Yiwei Ci, Qiusong Yang, Yufeng Li, Zhichao Lyu*
2247	2.7	Direction-Based Route Integrity Validation for Eavesdropping Prevention in NoC Systems *Hsuan-Yu Huang Huang, Kun-Chih Chen*
2568	2.7	A Low-Power, High-Resolution Capacitance to Digital Conversion Mechanism for Invasive Attacks *Harikrishnan Balagopal, Shiva Nejati, Hamidreza Esmaeili Taheri, Mitra Mirhassani*
2651	2.7	A Post-Fabrication Tunable TDC-PUF Using VG-SOT MRAM for Robust Hardware Security *Tianrui Guo, Bi Wang, Chao Wang, Zhaohao Wang*
2914	2.9	GT2N: An Open-Source 2nm Nanosheet PDK Enabling Multi-Width/VT Benchmarking *Dongwon Jang, Piyush Kumar, Md. Nahid Haque Shazon, Sabareesh Jeevan Ram, Alexei Svizhenko, Victor Moroz, Ahmet Ceyhan, Nischal Arkali Radhakrishna, Azad Naeemi*

Neural Signal Processing and Seizure Detection Session

Session Code:	**C1P-22**	**Date & Time:**	**Wednesday May 27, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Xiao Liu**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1291	6.6	Lightweight Multi-View EEG Seizure Detection with a Two-Stage Low-Power BFP FFT–NN Accelerator *Chi Ben, Youbin Luo, Zhenglin Gu, Kexin Tian, Heng Zhang, Yuxiang Fu, Li Li*
2844	6.7	Accurate and Efficient Seizure Prediction Using Legendre Memory Units *Danial Baharlouei, Alireza Ahrar, Maher Assaad, Mostafa Rahimi Azghadi, Amirali Amirsoleimani*
2943	6.8	Energy-Efficient Epileptic Seizure Prediction Using Spiking Neural Networks *Alexander Brady, Debra Moore-Hill, Fawad Khan, Hisham Daoud*



Neural Stimulation and Closed-Loop Systems Session

Session Code:	**C1P-23**	**Date & Time:**	**Wednesday May 27, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Jennifer Blain**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1819	6.3	DQ-MappingSort: Event-Driven Low-Power Spike-Sorting with Low-Bit Spatio-Temporal Encoding and Adaptive Cluster Mapping *Kaiji Liu, Ning Pu, Yue Zhong, Zhihua Wang, Hanjun Jiang*
2194	6.3	A 32-Channel Neural Stimulator with 30V Supply Range and Bootstrap Charge Balancing Switches *Jiarun Yuan, Chenwang Mo, Yong Lian, Yang Zhao*
2362	6.3	An Area-Efficient Neural Stimulator Chip Achieving 23V Voltage Compliance by 180nm BCD CMOS Process *Zherui Li, Cheng Han, Qijing Xiao, Weixiao Wang, Yunshan Zhang, Jun Zhou, Bo Zhao*
2623	6.3	A 16-Channel Monopolar-and-Bipolar Super-Reconfigurable Neurostimulation IC with Active Charge-Balancing and 12-V Voltage Compliance in Standard CMOS *Jiachen Sun, Ruijie Zhao, Pengfei Han, Dingfu He, Anxi Hu, Hongming Lyu*
2845	6.2	An Energy-Efficient Neurostimulator with Closed-Loop Boost Converter for Dynamic Supply Regulation *Quanbei Chang, Xiao Liu*

Sensors and SoCs for Cellular and Biochemical Analysis Session

Session Code:	**C1P-24**	**Date & Time:**	**Wednesday May 27, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Xu Liu**

Papers are listed in the order they will be presented.

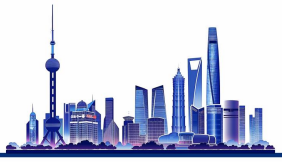
Paper Id	Topic	Title/Author
1376	6.3	A Low-Phase-Error FD-fNIRS Readout Circuit with Sub-1V Transimpedance Amplifier and LC-ADC-Based Amplitude Control Loop *Kangkang Xu, Shuo Zhang, Zheng Ding, Nan Zeng, Jian Zhao, Mohamad Sawan, Guoxing Wang, Cheng Chen*
1512	6.10	Neuromorphic Sensing-and-Computing for Multi-Panel Cancer Diagnostics by Memristive Biosensors *Junrui Chen, Sandro Carrara*
1613	6.5	FastDEP: A CMOS DEP Chip with Frequency and Voltage Scaling for Cell Biology Applications *Yu-Chen Chang, Lin-Hung Lai, Shao-Hua Lian, Yu-Chen Hung, Wen-Yue Lin, Bang-Yuan Xiao, Fang-Chen Lo, Chen-Yi Lee*
2144	6.5	A 64-Pixel CMOS-MEA with 8 Piezoelectric Sensor Readout Channels for Simultaneous Electrophysiology and Mechanobiology Cell Studies *Sam Sorrenti, Virgilio Valente*
2607	6.5	A Low-Power Tunable Dynamic-Range ISFET Sensor with In-Pixel Incremental ΣΔ Quantisation *Shuanghua Liu, Pantelis Georgiou*

Image and Vision Sensors II Session

Session Code:	**C1P-25**	**Date & Time:**	**Wednesday May 27, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Chen Shoushun, Jie Chen**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1349	7.10	Analysis of Photoreceptor Non-Linearity in Dynamic Vision Sensors *Yu Xin, Xiaopei Shi, Ruoyu Ji, Jiangtao Xu, Kaiming Nie*
1543	7.7	Time-of-Flight Extraction Using a Partial Temporal Attention Spiking Neural Network for SPAD-Based LiDAR *Hao Shi, Hao Zhang, Dong Li, Yaoqi Bao, Rui Ma, Zhangming Zhu, Yanfei Liu, Hao Zheng*
1542	7.10	A Fully Digital Dynamic Vision Sensor Based on Time to First Spike Encoding *Ayoub Talbi, Ali Naimi, Xavier Lesage, Marco Passy, Skandar Basrour, Laurent Fesquet*
1604	7.3	A Passive Threshold-Voltage-Mismatch Cancellation Technique for Visual-Neuron-Inspired HDR CMOS Image Sensors *Liang Shi, Yuchen Wang, Junhao He, Qinhan Xu, Jingjing Liu*
1755	7.9	A 4/8b High-Precision Fully-Parallel In-Sensor Computing Chip with Subthreshold Digital Pixel and Hybrid Pulse Modulation *Junda Zhao, Yimo Du, Taoyi Wang, He Zhang, Junzhan Liu, Liang Zhang, Wang Kang*
2035	7.10	Log-Normal FPN in DVS from Bias Mismatch *Xiaopei Shi, Ruoyu Ji, Yu Xin, Kaiming Nie, Jiangtao Xu*
2045	7.10	Exponential Distribution of DVS Events and High Latency Under Low Light *Ruoyu Ji, Xiaopei Shi, Yu Xin, Kaiming Nie, Jiangtao Xu*
2252	7.14	A LiDAR Point Cloud Dataset for Crowd Segmentation and Counting *Chaima Zaghouani, Abdullah Khanfor, Hakim Ghazzai, Ahmad Alsharoa, Gianluca Setti*
2273	7.11	Mid-Level LiDAR and Event-Based Vision Fusion for Robust 3D Perception *Mohamed Aziz Benhouichet, Charalampos Antoniadis, Hakim Ghazzai, Gianluca Setti*
2600	7.10	An Event-Driven E-Skin System with Dynamic Binary Scanning and Real Time SNN Classification *Gaishan Li, Zhengnan Fu, Anubhab Tripathi, Junyi Yang, Arindam Basu*
1536	7.14	FPGA Implementation of Sketched LiDAR for a 192 × 128 SPAD Image Sensor *Zhenya Zang, Mike Davies, Istvan Gyongy*
1767	7.14	A Shared-TDC Architecture for Large-Scale SPAD Arrays Enabling Range-Gated Timing in Flash LiDAR Sensors *Sadra Tafaghodi Jami, Ali Fotowat-Ahmady, Jie Yuan*
1883	7.14	Hardware-Efficient Image Super-Resolution for Solid-State LiDARs Using Single-Pixel Imaging *Yiyang Liu, Istvan Gyongy, Robert Henderson*
2044	7.14	A High-Accuracy Peak Detection Algorithm Using a First-and-Last-Event Histogram with a Dual-Mode TDC for dToF Sensors *Xiayu Wang, Chunlin Li, Jin Hu, Rui Ma, Dong Li, Zhangming Zhu*
1598	7.3	Near-Field Radar Imaging Acceleration Strategy Using Wavelet Transform and Multiscale Processing *Tianxing Lu, Yang Zhao, Yingjian Hao, Jingqian Wang, Leilei Huang, Chunqi Shi, Jinghong Chen, Runxi Zhang*



Sensory Circuits and Systems II Session

Session Code:	**C1P-26**	**Date & Time:**	**Wednesday May 27, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Navid Yazdi, Yuanqi Hu**

Papers are listed in the order they will be presented.

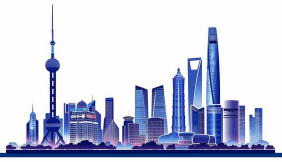
Paper Id	Topic	Title/Author
1212	7.6	A 5MHz-Bandwidth CMOS Hall Current Sensor with Non-Spun Voltage-Biased Hall Plates and SAR-Accumulator Offset Calibration *Yizhen Chen, Haoming Luo, Hong Chen, Ye Zheng, Yinuo Chen, Jinhang Sun, Junyu Wang, Rui Yin*
1645	7.1	An Artifact-Suppressing Neural Stimulator Using Differential Push-Pull Architecture *Minghao Zhong, Xu Liu*
1692	7.14	A Hybrid Quantization Method for FMCW Radar Data Compression *Yubo Guo, Leilei Huang, Chunqi Shi, Jinghong Chen, Runxi Zhang*
1919	7.1	Development of a Photoacoustic Platform for Blood Glucose Monitoring and a Comparative Study Between Signal Propagation Delay and Peak-to-Peak Amplitude *Jianyu Zhang, Zhizhang Li, Luohan Lin, Guoxing Wang, Cheng Chen*
2182	7.15	Ultra-Low Latency Synchronous Integral Demodulation Technique for Eddy Current Sensor *Jiaze Yu, Yixian Liu, Zongxue Yan, Jianzheng Li, Yajie Qin*
2505	7.16	A Static-Gradient, IC-Based 0.5-T NMR Spectrometer for 2D Diffusion–Relaxation Analysis of Solid Peanuts *Shuhao Fan, Jie Wang, Hefei Liu, Daniel Krüger, Yi-Qiao Song, Donhee Ham*
2565	7.4	Adaptive Federated Learning Defense Against Byzantine Attacks and Concept Drift in IIoT *Assem Alhelou, Amit Kumar Singh, Xiaohang Wang*
2591	7.15	Distributed Instrumented Paddle for Real-Time Kayak Performance Analysis: IACF-Based Cadence Estimation *Souebou Bouro, Antoine Courtay, Mickaël Le Gentil, Olivier Berder, Guillaume Nicolas, Nicolas Bideau*
2848	7.2	Multimodal Smart Insole with Crossbar Crosstalk Compensation for Fall-Risk Prediction *Junjian Chi, Zihuan Zhang, Qingyu Zhang, Andreas Demosthenous, Yu Wu*
1109	7.16	Integrated Current and Vibration Sensing System for Condition Monitoring of a Drone Docking Station *Manatsanan Trakulruangroj, Worameth Nantareekurn, Pattawut Manapongpun, Nopporn Bussabavalai, Prakarn Jaroonsorn, Thapanun Sudhawiyangkul, Theerawit Wilaiprasitporn, Poramate Manoonpong*
1234	7.5	Internet of Drones System for Water Quality Sensing, Sampling, 2-D Mapping, and 3-D Profiling *Soheyl Faghir Hagh, Parmida Amngostar, Tian Xia*
1406	7.11	Robust and Accurate Line Following Navigation by Hybrid Infrared-Visual Modes for Mobile Robots *Bohan Sun, Lin Xiao, Hao Xiong, Leilei Gu*
2525	7.10	A Mixed-Signal Gaussian-Based Super-Resolution Sensor Interface Circuit for High-Density Tactile Perception *Feiyang Chen, Zhiheng Huang, Pengcheng Zhu, Zuyang Cao, Bo Zhao, Yuxuan Luo*
2928	7.16	Fast Response Proximity and Tactile Sensory for Safe Human-Robot Collaboration *Tianyang Yao, Andreas Demosthenous*
1154	7.1	Screening of Lumbar Disc Herniation Using Buttock Pressure Imaging System *Jin Ai, Sixu Tao, Menghan Hu, Jian Zhang*

Semantic and Hardware-Aware Advances in 3D Vision Session

Session Code:	**C1P-27**	**Date & Time:**	**Wednesday May 27, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Dongmei Li**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1699	12.9	Semantic-Aware Sparsity and Adaptive Octree Partition for Efficient Deployment of Point Cloud Models on Edge Devices *Weigui Li, Le Qiu, Weichen Gao, Wenyu Sun, Yongpan Liu, Dongmei Li*
1777	12.9	SEGA-PointNet: A Semantic Enhancement and Global Aggregation Network for Maize Organ Segmentation from 3D Point Clouds *Liruizhi Jia, Xiaoyang Bi, Bo Kong, Yuan Liu, Kan Feng, Shengquan Liu*
1904	12.9	FPPS: An FPGA-Based Point Cloud Processing System *Xiaofeng Zhou, Linfeng Du, Hanwei Fan, Wei Zhang*
2332	12.9	Visual Geometric 6-DoF Grasping: A Multi-View Framework with Sparse RGB Observations *Yixiang Dai, Kaiqin Yang, Haoran Zhu, Ruiyang Li, Yongjiang Zhao, Xiaobing Feng, Huimin Ma, Siang Chen, Guijin Wang*



Analog and Mixed-Signal Circuit Design Techniques Session

Session Code:	**C4P-17**	**Date & Time:**	**Wednesday May 27, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Xi Zhu, Gordon Roberts**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1220	1.3	A 14-Bit 4GS/s DAC Achieving 68dBc SFDR Up to 1.7GHz with Digital Pre-Distortion and Switching-Glitch Compensation in 28nm CMOS Process *Junfeng Wang, Kejun Wu, Jun Liu, Shiteng Li, Qianfeng Zhang, Geyou Hu, Xin Duan, Zhen Yu, Ning Ning, Jing Li, Zhong Zhang, Qi Yu*
1312	1.8	Three-Level GaN HEMT Gate Driver with Negative VGS Pulse and Integrated Overcurrent Protection *Nick Van Houtven, Jef Thoné, Mike Wens, Valentijn De Smedt*
1689	1.8	A 2RW Dual-Port 8T-SRAM Macro with Bitline Leakage Current Tracking and Read-Write Arbitration *Chenghu Dai, Junbo Chen, Lian Liu, Zaihang Zhang, Licai Hao, Wei Hu, Chunyu Peng, Wenjuan Lu, Zhiting Lin, Xiulong Wu*
2917	1.8	A 0-400MHz DDFS Based on the Multi-Level CORDIC Pipeline for Radar Applications in 65-nm CMOS Process *Jiang Wu, Yiqing Wang, Buwen Liu, Guixiang Jin, Weifeng Sun, Zhongyuan Fang*

Mixed-Signal Building Blocks and Power-Efficient Analog Circuits Session

Session Code:	**C4P-18**	**Date & Time:**	**Wednesday May 27, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Bibhu Sahoo, Lei Zhang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1257	1.3	A 19.43-Bit Effective Resolution and 3.9 kSPS SAR-Based Integrator-Residue Extended Counting First-Order ΔΣ ADC *Sanghwa Han, Hyunjoong Lee, Nam Soo Kim, Jaehoon Jun*
1400	1.1	A Fully Open-Source Implementation of an Analog 8-PAM Demapper for High-Speed Communications *Mohamed Aiham Hemza, Alex Alvarado, Krzysztof Herman, Piyush Kaul*
1529	1.8	Low Supply, Impedance-Boosted Current Mirror Using Back-Gate in FD-SOI Technology *Roopesh G L, Arpan Jain, Soham Bhattacharyya, Ashfakh Huluvallay, Andleeb Zahra, Zia Abbas*
2540	1.1	A Comparative Study of Multilevel PWM Techniques with Circuit Non-Idealities in Class-D Audio Power Amplifiers *Chiara Rossini, Antonio Aprile, Elisabetta Moisello, Giuseppe Falcone, Francesco Rezzi, Edoardo Bonizzoni, Piero Malcovati*
2649	1.1	Design of a Class-J Power Amplifier with Reactive-Resistive Second Harmonic Termination for Improved Efficiency *Mahima Patel, Sujay S, Debarati Sen, Mrinal Kanti Mandal*

Modeling and Control of Power Converters, Energy Grids, and Systems Session

Session Code:	**C4P-19**	**Date & Time:**	**Wednesday May 27, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Zhen Li, Federico Bizzarri**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1473	4.10	A Profit Guranteed Dynamic Dual-Pricing Model and Robust Scheduling Approach for Electric Vehicle Charging in Microgrid *Shing Chow Chan, Mingyuan Wen, Ho Chun Wu*
2488	4.2	A 6.78MHz Dual Output Wireless Power Transfer System with Fast Transient Response and Adaptive Global Power Control *Junjie Fan, Min Sun, Haolu Xie, Xing Li*
1584	4.3	A Novel PFM Control Chip with Model-Based Duty Ratio Prediction and vds-Sensed Fine Tuning for Optimal ZVS in VHF Resonant SEPIC Converters *Weihua Zhang, Desheng Zhang, Run Min, Qiaoling Tong, Jianming Lei, Xuecheng Zou*
2000	4.3	Double-Clock Architecture for Small-Duty-Cycle DC-DC Converters *Mirko Alecci, Alessandro Gasparini, Claudio Bona, Edoardo Bonizzoni, Piero Malcovati, Alessandro Bertolini*
1301	4.8	A 97.4% Efficiency IoT Buck Converter with Adaptive On-Time and Quasi-V2 Control *Huajun Guo, Zhen Wang, Youlin Wu, Siyuan Li, Chenchang Zhan*
1591	4.8	Step-Down DC-DC Converters with Transient Enhancement Technique Based on Active Compensation for Large-Load Applications *Xiao Shu, Hiu Fung Fok, Bohang Zheng, Liang Zhou, Yong Zhou, Jianjun Zhou*
1744	4.8	A Symmetrical RHP-Zero-Free Hybrid Boost Converter with Eliminated Flying Capacitor Inrush Current and Enhanced Output Current Continuity *Zhitong Chen, Junyi Liu, Xingyuan Niu, Yudi Ren, Xiaoya Fan, Yanzhao Ma*
1898	4.8	A Buck Converter with Mixed-Signal Computational Charge Balance Control for One-Cycle Fast Recovery *Shiyuan Wang, Zekun Zhou, Yan Lu*
2465	4.8	A Compact Current Balancing Method for Multi-Phase Buck DC-DC Converter *Yining Wang, Min Sun, Haolu Xie, Xing Li*
2578	4.8	A Battery Management System Applied to Critical Remote Devices, Featuring High Transient Response and Battery-System Separate Charging *Xuanye Li, Minggang Chen, Wangchen Fan, Guorong Jiang, Zekai Tian, Weifeng Sun, Zhongyuan Fang*

Circuits and Systems for Power Converters, Energy Harvesting, and Wireless Power Transfer Session

Session Code:	**C4P-20**	**Date & Time:**	**Wednesday May 27, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Hirotaka Koizumi, Zhicong Huang**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1373	4.1	A 94.6% Peak-Efficiency 2-Phase 3-Level Buck Converter with Dual-Path Flying Capacitor Balancing and Novel Pre-Charging *Yani Li, Jin Zou, Kaijie Tang, Wei Xi, Zhangming Zhu*
1851	4.1	A 2.3-ns Response Time Temperature Insensitive Capacitive Level-Shifter with a Novel Active Pull-Up for a 100-V Monolithic GaN Half Bridge *Tommaso Francesco Tardani, Andrea Gambero, Stefano Corona, Sandro Rossi, Antonio Aprile, Elisabetta Moisello, Giulio Ricotti, Edoardo Bonizzoni, Piero Malcovati*
2254	4.1	A Feedforward-Feedback Reconfigurable Switched-Capacitor DC-DC Converter with One-Step VCR Transitions Achieving 9.6V/μs Under 5MHz Fast DVS for Edge AI Applications *Ya-Ting Hsu, Ke-Horng Chen, Chen-Yen Ho, Hou-Wei Teng, Hsiang-Hui Chang*
2758	4.1	A High-Efficiency Buck–Boost Converter with a Wide Load Range for Neural Stimulators *Zheyuan Fei, Tong Zhou, Wanyuan Qu*
2778	4.1	A 16-Phase High Frequency Integrated Voltage Regulator with On-Chip Current Sensing and Smooth Phase Shedding/Adding *Chi Zhang, Shaowei Zhen, Zuyue Pang, Chenguang Lv, Shuhai Chen, Xiaohuan You, Ziyi Cui, Luhao Cha, Bo Zhang*
2907	4.1	A Monolithic GaN Bidirectional Load Switch with Fast Turn-On Control and Inrush Current Protection *Ruize Sun, Yuxin Wang, Yuxiao Yang, Zekun Zhou, Wanjun Chen, Bo Zhang*
2076	4.4	A High dv/dt-Tolerant Level Shifter with Sub-Nanosecond Delay Using Dummy Pulse Protection *Zane Gunn, Daniel Truesdell, Benton Calhoun*
2317	4.4	A Monolithic GaN Active Gate Driver Achieving 71.6% Ringing Reduction Across Various Load Currents Using a Ringing Sensor and Simplified Digital Algorithm *Wenjia Xu, Huajun Zhang, Hesheng Lin, Guoqi Zhang, Qinwen Fan*
2950	4.4	A Charge-Recovery Half-Bridge Gate Driver with Discrete Feedback Timing Control Achieving Over 70% Power Reduction *Wentao Liu, Yunhong Zhu, Zhina Lian, Hao Min*
2881	4.5	S-SSHI/SECE Hybrid Circuit with Two Diodes for Piezoelectric Devices *Koshi Osawa, Wenqi Zhu, Hirotaka Koizumi*
1535	4.6	Experimental Validation of Irradiance Reconstruction and MPPT Performance for Offshore Floating Photovoltaic Systems *Hui Jin, Xiangyu Kong, Hongbin Liu*
2533	4.7	A Constant-Loss 6.78-MHz Wireless Power Transfer System with Hybrid Class-ED Power Amplifier for D2D Fast Charging *Jiwei Zou, Kai Cui, Yan Lu*
2626	4.7	A Gate-Biased Wide-Range Rectifier for Neural Stimulation *Cheng Han, Zhiwei Zhang, Jingna Mao*
2819	4.7	Receiver Localization for Deep-Implant Wireless Power Transfer System at 6.78MHz Using a Flexible Transmitter-Coil Array *Jiaxing Zhang, Dai Jiang, Andreas Demosthenous*
1928	4.7	Voltage-Controlled Delay Line for Precise Phase Tuning of a 10-MHz Clock in Integrated Dual Active Bridge Converters *Francesco Romano, Elisabetta Moisello, Alessandro Liotta, Pietro Giannelli, Giovanni Frattini, Edoardo Bonizzoni, Pie...*
1416	4.1	A Hybrid Single-Mode Buck-Boost Converter Using Lower-Voltage MOSFETs with Reduced Inductor Current and 95.8% Peak Efficiency *Yani Li, Runyu Zhu, Yifei Hua, Ji Bian, Zhangming Zhu*

Bio-Signal Acquisition Front-Ends and ADCs Session

Session Code:	**C4P-21**	**Date & Time:**	**Wednesday May 27, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Yu Wu**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1081	6.1	A Low Noise Bio-Potential AFE Achieving 300-mV EDO Tolerance and <20-ms-Settling with VCO-Based Full Digital DC Servo Loop *Shengping Lv, Guanzhe Hu, Liuxin Lv, Peng Zhang, Fei Chen, Wen Jia, Shuqiang Lu, Zhihua Wang, Hanjun Jiang*
1252	6.1	A Chopping Technique for High Input Impedance Biopotential Instrumentation Amplifiers *Alejandro David Fernandez Schrunder, Stéphane Emery, Amrith Sukumaran*
1852	6.4	Towards a High-Performance Capacitively Coupled Non-Contact ECG Acquisition System *Rui Liu, Heng Zhao, Xu Zhang, Huan Hu*
2838	6.3	Direct Neural ADC via Level-Crossing Quantization: Feasibility, Trade-Offs, and Design Guidelines *Mina Sayedi, Hossein Kassiri*

AI and Accelerators for Medical Imaging/Diagnostics Session

Session Code:	**C4P-22**	**Date & Time:**	**Wednesday May 27, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Riccardo Collu**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1039	6.8	BioSeek: A Design Generation Framework of Biosignal Processors with Large-Language Models for Edge Healthcare Applications *Fengshi Tian, Jiakun Zheng, Hui Wu, Zilu Liu, Jinbo Chen, Shiqi Zhao, Jie Yang, Mohamad Sawan, Chi-Ying Tsui, Kwang-Ting Cheng*
1292	6.4	SCOPE-3D: An Energy Efficient Accelerator for Implicit Neural Representation-Based Sparse-View Computed Tomography Reconstruction *Haochuan Wan, Haoyan Li, Xin Li, Qing Wu, Yuhan Gu, Wenyan Su, Yuyao Zhang, Xin Lou*
1664	6.8	Dual Graph Feature Learning for ADHD Diagnosis: Integrating Node and Edge Information in Brain Networks *Xiaotong Wang, Yibin Tang, Yuan Gao, Xiaojing Meng, Ying Chen*
1752	6.10	On the Implementation of Low-Cost Neural-Network Models for Cardiac Arrhythmia Detection *Fotios Tsipis, Nikolaos Kostakis, Georgios Karakonstantis*

Wearable and In-Vivo Sensing Systems Session

Session Code:	**C4P-23**	**Date & Time:**	**Wednesday May 27, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Jingna Mao**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1507	6.6	A Miniaturized In-Mouth pH Sensing System for Real-Time Intraoral Telemetry *Lukas Schulthess, Philipp Schilk, Julian Moosmann, Andrea Gubler, Christian Vogt, Florian Wegehaupt, Michele Magno*
2434	6.6	Wearable System with Real-Time Electrode Quality Evaluation for Continuous Long-Term ECG Monitoring *Shaimak Shukla, Anshu Sarje*
2534	6.3	A Dual-Stage ZOOM2 Light-to-Digital Converter for High-Dynamic-Range PPG Readout *Yinuo Chen, Hong Chen, Yanfei Sun, Yizhen Chen, Junyu Wang, Rui Yin*
2551	6.6	An Integrated Wearable Electromagnetic Sensing System with Wireless Vector Readout for Noninvasive Glucose Monitoring *Shiquan Wang, Boshen Xu, Wentao Wu, Yange Wang, Yuanjin Zheng*

Next-Generation Intelligent Sensors and Bio-Interfaces Session

Session Code:	**C4P-24**	**Date & Time:**	**Wednesday May 27, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Ibrahim Elfadel, Hong Chen**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1684	6.8	In-Sensor Computing by Reconfigurable Field-Effect Transistors *Junyan Qian, Roberta Grasso, Sandro Carrara*
1892	6.4	Broadband Microfluidic Coplanar Waveguide Biosensor for Position-Dependent Cell Detection *Jin Chen, Liangzun Fu, Xiwei Huang, Jiangtao Su, Ben Wang, Lingling Sun*
2663	6.4	A 4 nW 114 dB DR Electrochemical Sensing Interface IC with Digital-Intensive Regulation Loop *Muhammad Asfandyar Awan, Muhammad Haris Farooq, Amine Bermak, Muhammad Abrar Akram, Bo Wang*
2801	6.10	A Low Noise Electronic Platform for Monitoring and Stimulation of Biohybrid Machines *Riccardo Collu, Sonia Maxia, Usama Mahmood, Giulia Casula, Stefano Lai, Massimo Barbaro*
2998	6.6	Closed-Loop Arrhythmia Classification with Level-Crossing Sensing and Bidirectional SNN *Nhat Tri Vo, Hamid Rahimian Kalatehbali, Amirali Amirsoleimani, Yong Lian*

Neuromorphic Devices and Memristive Technologies Session

Session Code:	**C4P-25**	**Date & Time:**	**Wednesday May 27, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Xinming Shi**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1855	8.7	Analysis and Evolution of Dynamics in 1R Memristive Crossbars: From Sneak Currents to Analog Computing *Xinming Shi*
2811	8.7	Mixed-Mode ReRAM Architecture with Digital Weights and Inputs for High-Precision In-Memory Computing *Nithin Krishnan, Rajiv Joshi, Alex James*
1185	8.5	Novel M-CNN Design Fostering Gradual Switching of InGaZnO(IGZO)-Based Memristive Devices *Peijia Yuan, Kristoffer Schnieders, Yongmin Wang, Vasileios Ntinas, Maria Elias Pereira, Vikas Rana, Alon Ascoli, Ronald Tetzlaff, Regina Dittmann, Stephan Menzel*
1774	8.3	A Biomimetic Nanopore Memristor Model for Emulating Synaptic Plasticity in Neuromorphic Circuits *Mostafa Shooshtari, Saeideh Pahlavan, Teresa Serrano-Gotarredona, Juan Bisquert, Bernabé Linares-Barranco*
2603	8.6	A 40-nm Resilient MLC RRAM Macro with Self-Referenced Time-Based Readout and 3-Bit Interleaved ECC Achieving 0.22 pJ/Bit Read Energy *Junjie He, Zhen Kong, Yida Liang, Humiao Li, Yida Li, Jiamin Li, Longyang Lin*

Biomedical and Sensory Neural Systems Session

Session Code:	**C4P-26**	**Date & Time:**	**Wednesday May 27, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Yang Zhao**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1778	8.1	TF-MV SwAV++: Subject-Invariant Time–Frequency Prototype Learning for Cross-Subject sEEG Seizure Detection *Yunsheng Liao, Jie Yang, Mohamad Sawan*
2298	8.1	Variance-Aware Quantized Multi-Scale Conformer for Efficient ECG Rhythm Classification on Resource-Constrained Devices *Sudhanshu Gaurhar, Tushar Shinde, Surender Deora, Anil Kumar Tiwari*
2839	8.1	AEGIS-ES: Hazard-Adaptive Conformal Event-Sparse Inference for Glucose Monitoring *Zijia Wang, Christofer Toumazou*

Neural Network Hardware Accelerators Session

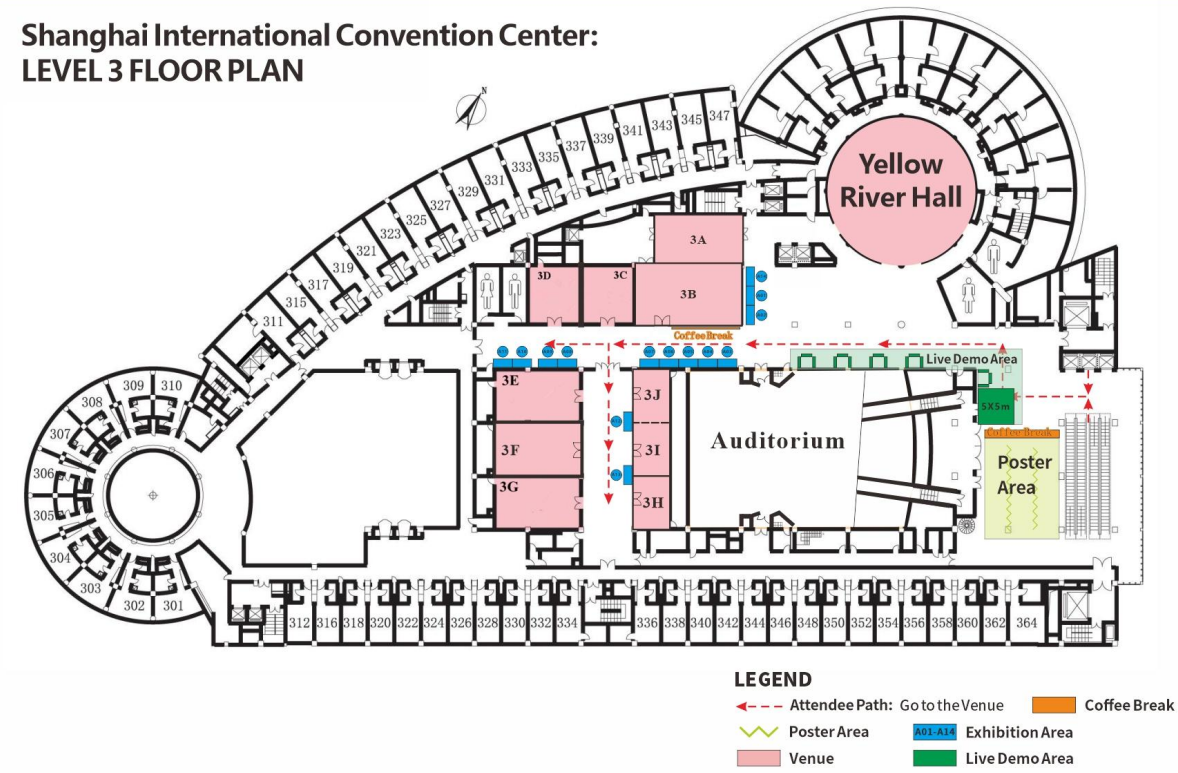
Session Code:	**C4P-27**	**Date & Time:**	**Wednesday May 27, 2026 (14:30 - 16:30)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Jim Harkin**

Papers are listed in the order they will be presented.

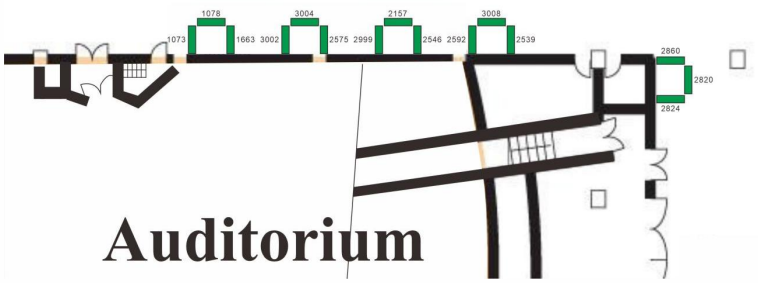
Paper Id	Topic	Title/Author
1580	8.2	A Layer-Aware Heterogeneous SNN Accelerator Architecture for Energy-Efficient Inference on Resource-Limited FPGAs *Zeyuan Song, Xingan Sha, Youhua Shi*
2757	8.2	An FPGA-Based SoC Architecture with a RISC-V Controller for Energy-Efficient Temporal-Coding Spiking Neural Networks *M Javad Sekonji, Ali Mahani, Maryam Mirsadeghi, Mahdi Taheri*
1316	8.2	A Configurable Energy-Efficient Dual-Mode Accelerator for DNN and SNN *Jingwei Zhu, Xinyang Wu, Jianghao Wu, Yun Chen*
1402	8.3	PIM-NoC: A NoC Architecture with In-Router Processing-in-Memory for DNN Acceleration *Yi Liu, Haixiang Ren, Lixia Han, Cuiyu Qi, Hui Chen, Yuxiang Fu, Li Li*
1765	8.1	SlimTTS: Parameter- and Compute-Efficient Neural Text-to-Speech Synthesis for Real-Time Inference *Arne de Beer, Chang Gao*
2239	8.2	SPEAR: Spike-Aware Point Pruning and Fused FPS–KNN Sampling for Spiking Point Transformer Acceleration Co-Design *Yilong Fang, Pinfeng Jiang, Letian Wang, Yi Wang, Mingde Zhu, Xiangshui Miao, Xingsheng Wang*
2885	8.4	Performance-Aware Design Space Exploration for Chiplet-Based Cortical Simulation Processors Considering Area Constraint *Fanxi Yang, Yi Zheng, Lufei Fan, Qi Jiang, Tianhao Li, Xun He, Li-Rong Zheng, Zhuo Zou*

Live Demo Assignments & Guidelines

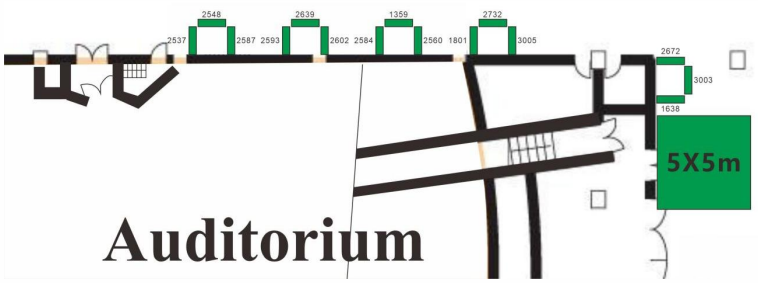
ISCAS 2026: CONFERENCE VENUE GUIDE



Monday, May 25th, 2026



Tuesday, May 26th, 2026



Station Assignment

1. Poster Specifications

- **Maximum Size:** 90cm (W)X 20cm (H).
- **Orientation:** Portrait (Vertical) orientation only.
- **Backboard Dimensions:** Each presenter is provided with a vertical display board measuring 1m (W) X2m (H).
- **Mounting Materials:** Adhesive tape will be provided on-site by the staff.

2. Live Demo Technical Specifications

- **Each demo table will be equipped with:**
- **Workstation:** One office table measuring 1.8m (Length) $\times$ 0.45m (Width).
- **Power Supply:** 220V / 50Hz (Standard China Power).
- **Outlet:** One multi-standard power strip.
- **Plug Compatibility:** Supports Plug Types A, C, and I (Standard two-flat, two-round, or three-flat pins).
- **Adaptors:** One international universal adaptor.

3. Venue & Environment

- **Location: SHICC Lobby, Level 3**
- **Internet Access:** Complimentary Wi-Fi is available. For high-bandwidth or stable wired Ethernet requirements, please contact the on-site staff.

4. Daily Schedule (May 25 – 26, 2026)

To ensure a smooth transition between sessions, please strictly follow the schedule below:

- **Morning Session: 10:00 – 12:00**
- **Set-up: 09:30 – 10:00**
- **Presentation: 10:00 – 12:00**
- **Teardown: 12:00 – 12:30**

5. Important Notes

- **Station Assignment:** Please refer to the layout map for station assignments. Simply locate your assigned spot on the map based on your Paper ID.
- **Removal:** Posters and equipment remaining after the 30-minute teardown window will be cleared by the PCO staff.

Live Demo Session Schedule- Detailed Agenda

Biomedical Live Demonstrations Session

Session Theme: Circuits & Systems for Medicine & Healthcare (MED)

Session Code:	**A1P-17**	**Date & Time:**	**Monday May 25, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Philipp Häfliger, Xilin Liu**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1073	16	Live Demonstration: A Portable Pressure Imaging System for Convenient and Ubiquitous Lumbar Disc Herniation Screening *Jin Ai, Sixu Tao, Menghan Hu, Jian Zhang*
1078	16	Live Demonstration: Flexible Airbag-Based Intraocular Pressure Monitoring System *Chaoyi Liu, Jiajie Chen, Longfei Li, Jiang Chang, Yue Wu, Jian Zhang, Menghan Hu*
1663	16	Live Demonstration: Low-Power Wearable System for Real-Time Myopia Prevention and Monitoring *Wanli Bai, Zhenguo Zhang, Jiajie Chen, Yunmian Li, Yue Wu, Menghan Hu*
3002	16	Live Demonstration: AI-Aided RF Reflectometry for Rapid Adulteration and Contamination Detection in Food Products *Temitope Odedeyi, Adeoluwa Oyinlola, Izzat Darwazeh*
3004	16	Live Demonstration: A Dual-Modal Neural Sensing Array System with Back-End Neural Signal Processing *Zepu Li, Songyu Han, Guoxing Wang, Yan Liu*
2575	16	Live Demonstration:A Reconfigurable and Self-Regulating Wearable NIRS Platform for Multi-Scenario Monitoring *Qianke Zeng, Nan Zeng, Shuo Zhang, Kangkang Xu, Zheng Ding, Yanyu Lu, Jian Zhao, Mohamad Sawan, Shan Fu, Guoxing Wang, Cheng Chen*
2999	16	Live Demonstration: A High-Resolution Plantar with Crosstalk Compensation for Human-Machine Interaction *Qingyu Zhang, Junjian Chi, Zihuan Zhang, Andreas Demosthenous, Yu Wu*

Live Demonstrations: Security and Trust Session

Session Code:	**A1P-18**	**Date & Time:**	**Monday May 25, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Philipp Häfliger,Xilin Liu**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2157	16	Live Demonstration: A 0.787pJ/Bit, 25 Mbps True Random Number Generator Based on Analog Chaotic Tent Map *Ruiqi Bao, Yuan Cao, Zheng Wan, Zhao Huang, Guangjun Yin*
2546	16	Live Demonstration: A Self-Adapting Randomness Extractor for a Monolithic QRNG *Andrea Bonzi, Nicola Massari, Luca Parmesan, Fabio Acerbi, Aymane Bouzafour, Marc Renaudin, Leonardo Gasparini*
2592	16	Live Demonstration: Hardware-Bound IP Protection for OWL-ViT on Edge Devices *Peichun Hua, Hanxiu Zhang, Tuo Li, Yue Zheng, Wenye Liu*
3008	16	Live Demonstration: Pocket-Size USB–C TRNG with Interactive GUI for High-Entropy Security *Berkay Özbek, Timothy Constandinou*

Live Demonstrations: RF Session

Session Code:	**A1P-19**	**Date & Time:**	**Monday May 25, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Philipp Häfliger, Xilin Liu**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2539	16	Live Demonstration: A 1TX/4RX Radar with Frequency-Dimension Virtual Aperture Expansion *Ruilin Liao, Haoran Wang, Jingzhi Zhang, Wei-Han Yu, Yue Song, Hongyang An, Huihua Liu, Kai Kang*
2814	16	Live Demonstration: MADA - An Interactive Multi-Agent Design Assistant for Radio-Frequency Integrated Circuits *Ignacio Gris, Jinru Duan, Zining Wang, Jian Gao, Xuan Zhang*
2820	16	Live Demonstration: Semi-Static Magnetic Field Localization System for Wireless Power Transfer *Jiaxing Zhang, Tianyang Yao, Dai Jiang, Andreas Demosthenous*
2860	16	Live Demonstration: A Flexible and Upgradable GNSS Receiver on Venus Architecture *Yule Jiao, Shiji Ruan, Limin Jiang, Zhiyuan Jiang, Shan Cao*

Classification & Object Recognition Live Demonstrations Session

Session Theme: AI in Circuits and Systems (AIC)

Session Code:	**B1P-17**	**Date & Time:**	**Tuesday May 26, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chair:**	**Peilin Liu**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
2537	16	Live Demonstration: Circular Object Recognition with Binary-Weight Spiking Neural Networks *Ryoichi Yuki, Oliver Velasco-Cardenas, Ayane Matsuzaki, Yoshinari Wada, Seiji Adachi, Kota Ando, Tetsuya Asai, Takao Marukame*
2548	16	Live Demonstration: Real Time Texture Classification on FPGA Using PVDF-Based Tactile Sensing *Riccardo Testa, Federico Manca, Mohamad Yaacoub, Francesco Ratto, Francesca Palumbo, Maurizio Valle*
2587	16	Live Demonstration: Real-Time Event-Based Daily Human Action Recognition with On-Chip Learning on ANP-I *Yahui Li, Jilin Zhang, Hong Chen*
2593	16	Live Demonstration: Transformer-Based Visual Object Detection and Tracking on MPSoC *Martín Romero Romero, Manuel Bendaña, Pablo Gil-Pérez, Daniel Cores, Fernando Pardo, Víctor Brea, Manuel Mucientes*
2639	16	Live Demonstration: An Efficient and Compact Visuo-Tactile Perception System *Cheng Qu, Erxiang Ren, Yonghua Li, Li Luo, Bin Fang, Guangyuan Xu, Fei Qiao*
2602	16	Live Demonstration: An Event-Driven E-Skin System with Dynamic Binary Scanning and Real Time SNN Classification *Zhengnan Fu, Gaishan Li, Anubhab Tripathi, Arindam Basu*
2584	16	Live Demonstration: A Personalized sEMG Gesture Recognition System Based on On-Chip Learning Neuromorphic Processor *Xijie Li, Jilin Zhang, Hong Chen*

Live Demonstrations: Intelligent Circuit Design and Fabrication Tools Session

Session Code:	**B1P-18**	**Date & Time:**	**Tuesday May 26, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Peilin Liu, Philipp Häfliger**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1359	16	Live Demonstration: A Vertically-Integrated Toolbox for the Simulation of ΣΔ Modulators *Francisco Gómez-Pulido, Javier Gallardo, Ismael Galán, Karim Sabra, Hampus Malmberg, Gustavo Liñán-Cembrano, José de la Rosa*
2560	16	Live Demonstration: Multi-Modal Agent for Interactive Multi-Process I/O Ring Generation *Zhishuai Zhang, Zengchun Chen, Xintian Li, Shilong Liu, Aodong Zhang, Lu Jie, Nan Sun*
2672	16	Live Demonstration: An Agile FPGA-Overlayed CGRA SoC for High-Efficiency Computing *Jiahang Lou, Jianrong Zhang, Yuan Dai, Zewei Zhong, Huan Lin, Wenbo Yin, Lingli Wang*
3003	16	Live Demonstration: The Hacker Fab Maskless Photolithography Stepper *Joel Gonzalez, Yanbing Chen, Jay Kunselman, John Wirant, Elio Bourcart, Matthew Moneck, Tathagata Srimani, Larry Pileggi*

Live Demonstrations: Sensory and Distributed Systems Session

Session Code:	**B1P-19**	**Date & Time:**	**Tuesday May 26, 2026 (10:00 - 12:00)**
Location:	**SHICC Lobby, Level 3**	**Chairs:**	**Peilin Liu, Xilin Liu**

Papers are listed in the order they will be presented.

Paper Id	Topic	Title/Author
1638	16	Live Demonstration: An Energy-Efficient SoC for Correlative Scan Matching Based 2D-LiDAR SLAM *Yulong Tan, Zixuan Shen, Jipeng Wang, Bingqiang Liu, Zhigang Wu, Lin Jiang, Chao Wang*
1801	16	Live Demo of a Bidirectional Communication Gateway for Battery-Free IoT End Devices *Yilin Wang, Junrui Liang*
2732	16	Live Demonstration: A Photovoltaic Asynchronous Time-Based Image Sensor *Pablo Fernández-Peramo, Sergio Palomeque-Mangut, Raquel Blanco-Suárez, Ángel Rodríguez-Vázquez, Juan Antonio Leñero-Bardallo*
3005	16	Live Demonstration: Capacitive Proximity Imaging Array for Human-Robot Interaction and Safety *Tianyang Yao, Jiaxing Zhang, Andreas Demosthenous*

CAS
IEEE CIRCUITS AND SYSTEMS SOCIETY

IEEE

ISCAS 2027

IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS
ISCAS 2027
BORDEAUX - FRANCE
6-9 JUNE

Promote your research at the **premier CAS conference**

CALL FOR TECHNICAL CONTRIBUTIONS

The IEEE International Symposium on Circuits and Systems (ISCAS) is the flagship conference of the IEEE Circuits and Systems Society and the world's premier forum for researchers working on the theory, design, and implementation of circuits and systems.

ISCAS 2027 will be held in Bordeaux, France, from 6 to 9 June 2027, and will feature a technical program including **regular papers (oral and poster presentations), special sessions, tutorials,** and **live demonstrations**, about emerging topic discussions.

SCOPE OF CONTRIBUTIONS

Submissions are invited in all areas of Circuits and Systems, including but not limited to:

- Analog and Mixed-Signal Circuits and Systems
- Digital Integrated Circuits and Systems
- Power and Energy Circuits and Systems
- Sensory Circuits and Systems
- Nonlinear Systems and Circuit Theory
- Digital Signal Processing
- Multimedia Systems and Applications
- Communications Circuits and Systems
- Biomedical Circuits and Systems
- Neural Networks and Neuromorphic Engineering
- High-Performance Computing for AI
- Circuits and Systems for Quantum Computing
- Beyond CMOS: Nanoelectronics and Heterogeneous Integration
- Education in Circuits and Systems

TYPES OF CONTRIBUTIONS

- **REGULAR PAPERS:** original research contributions to the state-of-the-art in circuits and systems.
- **SPECIAL SESSIONS:** proposals focusing on emerging, interdisciplinary, or high-impact topics that complement the regular program.
- **TUTORIALS:** short course or half-day educational sessions covering emerging trends or established techniques of practical and industrial relevance.
- **LIVE DEMONSTRATIONS:** interactive demonstrations of working systems (hardware and/or software), allowing attendees to directly experience and engage with the presented technologies.

IMPORTANT DATES

1. **SPECIAL SESSION PROPOSAL** Submission Deadline: **11 September 2026**
2. **REGULAR AND SPECIAL SESSION PAPER** Submission Deadline: **13 October 2026**
3. **TUTORIAL PROPOSAL** Submission Deadline: **13 October 2026**
4. **LIVE DEMONSTRATION** Submission Deadline: **13 October 2026**

PUBLICATION

Accepted papers will be included in the **ISCAS 2027 Proceedings** and submitted to **IEEE Xplore**. Selected papers will be invited for **journal extensions in leading IEEE CAS publications**.

ORGANIZING COMMITTEE

GENERAL CO-CHAIRS

Nathalie DELTIMPLE
(Bordeaux INP, France)
Francois RIVET
(University of Bordeaux, France)

TECHNICAL PROGRAM COMMITTEE CHAIRS

Thierry TARIS
(Bordeaux INP, France)
Malgorzata CHRZANOWSKA-JESKE
(Portland State University, USA)
Erika COVI
(University of Groningen, The Netherlands)
Hanho LEE
(Inha University, South Korea)

TUTORIAL CHAIRS

Antoine FRAPPE
(University of Lille – Junia, France)
Sara GHOREISHIZADEH
(Imperial College London, United Kingdom)
Qiang LI
(Hamburg University of Technology, Germany)
Nicole McFARLANE
(University of Tennessee, USA)

SPECIAL SESSION CHAIRS

Patricia DESGREYS
(Telecom Paris, France)
Sylvain BOURDEL
(Grenoble INP, France)
Hadi HEIDARI
(University of Glasgow, United Kingdom)
Marian VERHELST
(KU Leuven, Belgium)

LIVE DEMONSTRATIONS CHAIRS

Hamida HALLIL
(University of Bordeaux, France)
Jennifer HASLER
(Georgia Institute of Technology, USA)
Kea-Tiong TANG
(National Tsing Hua University, Taiwan)

FINANCE CHAIRS

Magali DEMATOS
(University of Bordeaux, France)
Yann DEVAL
(University of Bordeaux, France)
Mounir BOUKADOUM
(Université du Québec à Montréal, Canada)
Yoshifumi NISHIO
(Tokushima University, Japan)

LOCAL ARRANGEMENT CHAIRS

Marina DENG
(University of Bordeaux, France)
Jonathan SAUSSEREAU
(Bordeaux INP, France)

WEBSITE

https://2027.ieee-iscas.org/